

## General Description

The SN74HC/HCT259 is an 8-bit addressable latch. The device features four modes of operation. In the addressable latch mode, data on the D input is written into the latch addressed by the inputs A0 to A3. The addressed latch will follow the data input, non-addressed latches will retain their previous states. In memory mode, all latches retain their previous states and are unaffected by the data or address inputs. In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the D input and all other outputs are LOW. In the reset mode, all outputs are forced LOW and unaffected by the data or address inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## Features

- Input levels:  
For SN74HC259: CMOS level  
For SN74HCT259: TTL level
- Combined demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Specified from -40C to +125C
- Packaging information: DIP16/SOP16/TSSOP16

## Order Information

DEVICE	Package Type	MARKING	Packing	Packing QTY
SN74HC259N	DIP-16	74HC259N	Tube	1000/Box
SN74HC259DTR	SOP-16	74HC259	Tape	2500/Reel
SN74HCT259DTR	SOP-16	74HCT259	Tape	2500/Reel
SN74HCT259TDTR	TSSOP-16	74HCT259	Tape	3000/Reel

# Block Diagram And Pin Description

## Block Diagram

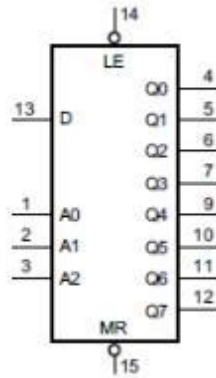


Figure 1. Logic symbol

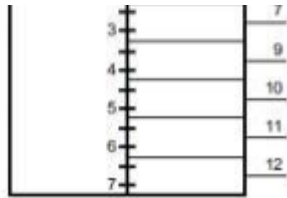


Figure 2. Functional diagram

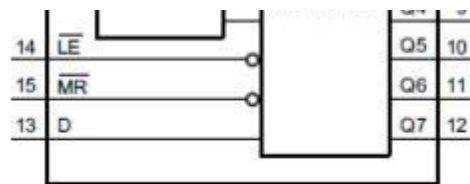
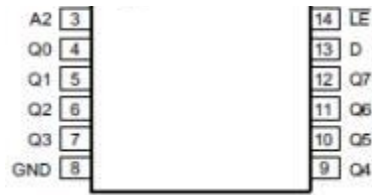


Figure 3. Functional diagram

**Pin Configurations**

**Pin Description**

Pin No.	Pin Name	Description
1	A0	address input
2	A1	address input
3	A2	address input
4	Q0	latch output
5	Q1	latch output
6	Q2	latch output
7	Q3	latch output
8	GND	ground (0V)
9	Q4	latch output
10	Q5	latch output
11	Q6	latch output
12	Q7	latch output
13	D	data input
14	$\bar{L}E$	latch enable input (active LOW)
15	$\bar{M}R$	conditional reset input (active LOW)
16	V <sub>CC</sub>	supply voltage

**Function Table**

Operating mode	Input						Output							
	MR	LE	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Reset (clear)	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active HIGH 8-channel decoder (when D=H))	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
Memory	H	H	X	X	X	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>

(no action)															
Addressable latch	H	L	d	L	L	L	Q=d	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
	H	L	d	H	L	L	q <sub>0</sub>	Q=d	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
	H	L	d	L	H	L	q <sub>0</sub>	q <sub>1</sub>	Q=d	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
	H	L	d	H	H	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	Q=d	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
	H	L	d	L	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	Q=d	q <sub>5</sub>	q <sub>6</sub>	q <sub>7</sub>	
	H	L	d	H	L	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	Q=d	q <sub>6</sub>	q <sub>7</sub>	
	H	L	d	L	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	Q=d	q <sub>7</sub>	
	H	L	d	H	H	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	q <sub>4</sub>	q <sub>5</sub>	q <sub>6</sub>	Q=d	

Note:[1]H= HIGHvoltagelevel;L=LOWvoltagelevel; X=don't care.

[2] d=HIGH or LOW data one set-up time prior to the LOW-to-HIGH  $\overline{LE}$  transition.

[3] q=lower case letter indicates the state of the referenced input one set-up time prior to the LOW -to-HIGH transition.

### Operating Mode Select Table

LE	MR	Mode
L	H	Addressable latch mode
H	H	Memory mode
L	L	Demultiplexer mode
H	L	Reset mode

Note: H=HIGH voltage level; L=LOW voltage level.

## Electrical Parameter

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Max	Unit
supply voltage	V <sub>CC</sub>	-	-0.5	+7 0	V
input clamping current	I <sub>IK</sub>	V <sub>I</sub> < -0.5V or V <sub>I</sub> > V <sub>CC</sub> +0.5V	-	±20	mA
output clamping current	I <sub>OK</sub>	V <sub>O</sub> < -0.5V or V <sub>O</sub> > V <sub>CC</sub> +0.5V	-	±20	mA
output current	I <sub>O</sub>	V <sub>O</sub> = -0.5V to (V <sub>CC</sub> +0.5V)	-	±25	mA
supply current	I <sub>CC</sub>	-	-	+70	mA
ground current	I <sub>GND</sub>	-	-70	-	mA
storage temperature	T <sub>stg</sub>	-	-65	+150	°C
total power dissipation	P <sub>tot</sub>	-	-	500	mW
Soldering temperature	T <sub>L</sub>	10s	DIP		C
			SOP/ TSSOP		260

**Recommended Operating Conditions**

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
SN74H259						
supply voltage	$V_{CC}$	-	2.0	5.0	6.0	V
input voltage	$V_I$	-	0	-	$V_{CC}$	V
output voltage	$V_O$	-	0	-	$V_{CC}$	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	$T_{amb}$	-	-40	-	+125	C
SN74HCT259						
supply voltage	$V_{CC}$	-	4.5	5.0	5.5	V
input voltage	$V_I$	-	0	-	$V_{CC}$	V
output voltage	$V_O$	-	0	-	$V_{CC}$	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	-	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	-	ns/V
ambient temperature	$T_{amb}$	-	-40	-	+125	C

**Electrical Characteristics**
**DC Characteristics 1**

 (  $T_{amb}=25\text{C}$ , voltages are referenced to GND ( ground=0 V ), unless otherwise specified. )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC259							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=2.0V$	1.5	1.2	-	V	
		$V_{CC}=4.5V$	3.15	2.4	-	V	
		$V_{CC}=6.0V$	4.2	3.2	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC}=2.0V$	-	0.8	0.5	V	
		$V_{CC}=4.5V$	-	2.1	1.35	V	
		$V_{CC}=6.0V$	-	2.8	1.8	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	2.0	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	6.0	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.98	4.32	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.48	5.81	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=2.0V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	0	0.1	V
			$I_O=4.0mA; V_{CC}=4.5V$	-	0.15	0.26	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	0.16	0.26	V
input leakage current	$I_I$	$V_I=V_{CC} \text{ or } GND; V_{CC}=6.0V$	-	-	$\pm 1.0$	$\mu A$	
supply current	$I_{CC}$	$V_I=V_{CC} \text{ or } GND; I_O=0A; V_{CC}=6.0V$	-	-	8.0	$\mu A$	
input	$C_I$	-	-	3.5	-	pF	

capacitance							
SN74HCT259							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=4.5V$ to $5.5V$		2.0	1.6	-	V
LOW-level input voltage	$V_{IL}$	$V_{CC}=4.5V$ to $5.5V$		-	1.2	0.8	V
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC}=4.5V$	$I_O=-20\mu A$	4.4	4.5	-	V
			$I_O=-4.0mA$	3.98	4.32	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_O=20\mu A$ ; $V_{CC}=4.5V$	-	0	0.1	V
			$I_O=5.2mA$ ; $V_{CC}=6.0V$	-	0.15	0.26	V
input leakage current	$I_I$	$V_I=V_{CC}$ or GND; $V_{CC}=5.5V$		-	-	$\pm 1.0$	$\mu A$
supply current	$I_{CC}$	$V_I=V_{CC}$ or GND; $I_O=0A$ ; $V_{CC}=5.5V$		-	-	8.0	$\mu A$
supply current	$\Delta I_{CC}$	$V_I=V_{CC}-2.1V$ ; other inputs at $V_{CC}$ or GND; $I_O=0A$ ; $V_{CC}=4.5V$ to $5.5V$	pin An, LE	-	150	540	$\mu A$
			pin D	-	120	432	$\mu A$
			pin MR	-	75	270	$\mu A$
input capacitance	$C_I$	-		-	3.5	-	pF

**DC Characteristics 2**

( $T_{amb}=-40^{\circ}C$  to  $+85^{\circ}C$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC259							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=2.0V$	1.5	-	-	V	
		$V_{CC}=4.5V$	3.15	-	-	V	
		$V_{CC}=6.0V$	4.2	-	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC}=2.0V$	-	-	0.5	V	
		$V_{CC}=4.5V$	-	-	1.35	V	
		$V_{CC}=6.0V$	-	-	1.8	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_O=-20\mu A$ ; $V_{CC}=2.0V$	1.9	-	-	V
			$I_O=-20\mu A$ ; $V_{CC}=4.5V$	4.4	-	-	V
			$I_O=-20\mu A$ ; $V_{CC}=6.0V$	5.9	-	-	V
			$I_O=-4.0mA$ ; $V_{CC}=4.5V$	3.84	-	-	V
			$I_O=-5.2mA$ ; $V_{CC}=6.0V$	5.34	-	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_O=20\mu A$ ; $V_{CC}=2.0V$	-	-	0.1	V
			$I_O=20\mu A$ ; $V_{CC}=4.5V$	-	-	0.1	V
			$I_O=20\mu A$ ; $V_{CC}=6.0V$	-	-	0.1	V
			$I_O=4.0mA$ ; $V_{CC}=4.5V$	-	-	0.33	V
			$I_O=5.2mA$ ; $V_{CC}=6.0V$	-	-	0.33	V
input leakage current	$I_I$	$V_I=V_{CC}$ or GND; $V_{CC}=6.0V$	-	-	$\pm 1.0$	$\mu A$	
supply current	$I_{CC}$	$V_I=V_{CC}$ or GND; $I_O=0A$ ; $V_{CC}=6.0V$	-	-	80	$\mu A$	
input capacitance	$C_I$	-	-	-	-	pF	
SN74HCT259							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=4.5V$ to $5.5V$	2.0	-	-	V	

LOW-level input voltage	$V_{IL}$	$V_{CC}=4.5V \text{ to } 5.5V$		-	-	0.8	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL};$ $V_{CC}=4.5V$	$I_O=-20\mu A$	4.4	-	-	
			$I_O=-4.0mA$	3.84	-	-	
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=4.5V$	-	-	0.1	
			$I_O=5.2mA; V_{CC}=6.0V$	-	-	0.33	
input leakage current	$I_I$	$V_I=V_{CC} \text{ or } GND; V_{CC}=5.5V$		-	-	$\pm 1.0$	
supply current	$I_{CC}$	$V_I=V_{CC} \text{ or } GND; I_O=0A; V_{CC}=5.5V$		-	-	80	
additional supply current	$\Delta I_{CC}$	$V_I=V_{CC}-2.1V;$ other inputs at $V_{CC}$ or $GND; I_O=0A;$ $V_{CC}=4.5V \text{ to } 5.5V$	pin An, LE	-	-	675	
			pin D	-	-	540	
			pin MR	-	-	338	
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC259							
input capacitance	$C_I$	D to Qn; see Figure 5	$V_{CC}=2.0V$	-	58	185	ns
			$V_{CC}=4.5V$	-	21	37	ns
			$V_{CC}=5.0V; C_L=15pF$	-	18	-	ns
input capacitance	$C_I$	-		-	-	-	

### DC Characteristics 3

( $T_{amb}=-40C$  to  $+125C$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC259							
HIGH-level input voltage	$V_{IH}$	$V_{CC}=2.0V$	1.5	-	-	V	
		$V_{CC}=4.5V$	3.15	-	-	V	
		$V_{CC}=6.0V$	4.2	-	-	V	
LOW-level input voltage	$V_{IL}$	$V_{CC}=2.0V$	-	-	0.5	V	
		$V_{CC}=4.5V$	-	-	1.35	V	
		$V_{CC}=6.0V$	-	-	1.8	V	
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	-	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	-	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	-	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.7	-	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.2	-	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH} \text{ or } V_{IL}$	$I_O=20\mu A; V_{CC}=2.0V$	-	-	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	-	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	-	0.1	V
			$I_O=4.0mA; V_{CC}=4.5V$	-	-	0.4	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	-	0.4	V
input leakage current	$I_I$	$V_I=V_{CC} \text{ or } GND; V_{CC}=6.0V$		-	-	$\pm 1.0$ uA	
supply current	$I_{CC}$	$V_I=V_{CC} \text{ or } GND; I_O=0A; V_{CC}=6.0V$		-	-	160 uA	
input capacitance	$C_I$	-		-	-	pF	
SN74HCT259							

HIGH-level input voltage	$V_{IH}$	$V_{CC}=4.5V$ to $5.5V$		2.0	-	-	V
LOW-level input voltage	$V_{IL}$	$V_{CC}=4.5V$ to $5.5V$		-	-	0.8	V
HIGH-level output voltage	$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC}=4.5V$	$I_o=-20\mu A$	4.4	-	-	V
			$I_o=-4.0mA$	3.7	-	-	V
LOW-level output voltage	$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_o=20\mu A$ ; $V_{CC}=4.5V$	-	-	0.1	V
			$I_o=5.2mA$ ; $V_{CC}=6.0V$	-	-	0.4	V
input leakage current	$I_I$	$V_I=V_{CC}$ or GND; $V_{CC}=5.5V$		-	-	$\pm 1.0$	$\mu A$
supply current	$I_{CC}$	$V_I=V_{CC}$ or GND; $I_o=0A$ ; $V_{CC}=5.5V$		-	-	160	$\mu A$
additional supply current	$\Delta I_{CC}$	$V_I=V_{CC}-2.1V$ ; other inputs at $V_{CC}$ or GND; $I_o=0A$ ; $V_{CC}=4.5V$ to $5.5V$	pin An, $\bar{LE}$	-	-	735	$\mu A$
			pin D	-	-	588	$\mu A$
			pin MR	-	-	368	$\mu A$
input capacitance	$C_i$	-		-	-	-	pF

**AC Characteristics 1**

 ( $T_{amb}=25^\circ C$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

propagation delay	$t_{pd}$	An to Qn; see Figure 6	$V_{CC}=6.0V$	-	17	31	ns
			$V_{CC}=2.0V$	-	58	185	ns
			$V_{CC}=4.5V$	-	21	37	ns
			$V_{CC}=5.0V$ ; $C_L=15pF$	-	17	-	ns
		$\bar{LE}$ to Qn; see Figure 7	$V_{CC}=6.0V$	-	17	31	ns
			$V_{CC}=2.0V$	-	55	170	ns
			$V_{CC}=4.5V$	-	20	34	ns
			$V_{CC}=5.0V$ ; $C_L=15pF$	-	17	-	ns
HIGH to LOW propagation delay	$t_{PHL}$	$\bar{MR}$ to Qn; see Figure 8	$V_{CC}=2.0V$	-	50	155	ns
			$V_{CC}=4.5V$	-	18	31	ns
			$V_{CC}=5.0V$ ; $C_L=15pF$	-	15	-	ns
			$V_{CC}=6.0V$	-	14	26	ns
transition time	$t_t$	see Figure 7	$V_{CC}=2.0V$	-	19	75	ns
			$V_{CC}=4.5V$	-	7	15	ns
			$V_{CC}=6.0V$	-	6	13	ns
pulse width	$w$	$\bar{LE}$ HIGH or LOW; see Figure 7	$V_{CC}=2.0V$	70	17	-	ns
			$V_{CC}=4.5V$	14	6	-	ns
			$V_{CC}=6.0V$	12	5	-	ns
		$\bar{MR}$ LOW; see Figure 8	$V_{CC}=2.0V$	70	17	-	ns
			$V_{CC}=4.5V$	14	6	-	ns
			$V_{CC}=6.0V$	12	5	-	ns
set-up time	$t_{su}$	D, An to $\bar{LE}$ ; see Figure 9 and Figure 10	$V_{CC}=2.0V$	80	19	-	ns
			$V_{CC}=4.5V$	16	7	-	ns
			$V_{CC}=6.0V$	14	6	-	ns
hold time	$t_h$	D to $\bar{LE}$ ; see Figure 9	$V_{CC}=2.0V$	0	-19	-	ns
			$V_{CC}=4.5V$	0	-6	-	ns



		and Figure 10	$V_{CC}=6.0V$	0	-5	-	ns
		An to $\overline{LE}$ ; see Figure 9 and Figure 10	$V_{CC}=2.0V$	2	-11	-	ns
			$V_{CC}=4.5V$	2	-4	-	ns
			$V_{CC}=6.0V$	2	-3	-	ns
power dissipation capacitance	$C_{PD}$	$f_i=1MHz; V_i=GND \text{ to } V_{CC}$		-	19	-	pF
<b>SN74HCT259</b>							
propagation delay	$t_{pd}$	D to Qn; see Figure 5	$V_{CC}=4.5V$	-	23	39	ns
			$V_{CC}=5.0V; C_L=15pF$	-	20	-	ns
		An to Qn; see Figure 6	$V_{CC}=4.5V$	-	25	41	ns
			$V_{CC}=5.0V; C_L=15pF$	-	20	-	ns
LE to Qn; see Figure 7	$V_{CC}=4.5V$	-	22	38	ns		
	$V_{CC}=5.0V; C_L=15pF$	-	20	-	ns		
HIGH to LOW propagation delay	$t_{PHL}$	$\overline{MR}$ to Qn; see Figure 8	$V_{CC}=4.5V$	-	23	39	ns
			$V_{CC}=5.0V; C_L=15pF$	-	20	-	ns
transition time	$t_t$	$V_{CC}=4.5V$ ; see Figure 7		-	7	15	ns
pulse width	$t_w$	$\overline{LE}$ HIGH or LOW; $V_{CC}=4.5V$ ; see Figure 7		19	11	-	ns
		MR LOW; $V_{CC}=4.5V$ ; see Figure 8		18	10	-	ns
set-up time	$t_{su}$	D, An to $\overline{LE}$ ; $V_{CC}=4.5V$ ; see Figure 9 and Figure 10		17	10	-	ns
hold time	$t_h$	D to $\overline{LE}$ ; $V_{CC}=4.5V$ ; see Figure 9 and Figure 10		0	-8	-	ns
		An to $\overline{LE}$ ; $V_{CC}=4.5V$ ; see Figure 9 and Figure 10		0	-4	-	ns
power dissipation capacitance	$C_{PD}$	$f_i=1MHz; V_i=GND \text{ to } V_{CC}-1.5V$		-	19	-	pF

Note:

[ 1] Typical values are measured at nominal supply voltage ( $V_{CC}=3.3V$  and  $V_{CC}=5.0V$ ). [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in uW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$ =input frequency in MHz;

$f_o$ =output frequency in MHz;

$C_L$ =output load capacitance in pF;

$V_{CC}$ =supply voltage in V;

$N$ =number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

**AC Characteristics 2**

 (T<sub>amb</sub>=-40C to +85C, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
<b>SN74HC259</b>							
propagation delay	t <sub>pd</sub>	D to Qn; see Figure 5	V <sub>CC</sub> =2.0V	-	-	230	ns
			V <sub>CC</sub> =4.5V	-	-	46	ns
			V <sub>CC</sub> =5.0V; C <sub>L</sub> = 15pF	-	-	-	ns
		An to Qn; see Figure 6	V <sub>CC</sub> =6.0V	-	-	39	ns
			V <sub>CC</sub> =2.0V	-	-	230	ns
			V <sub>CC</sub> =4.5V	-	-	46	ns
			V <sub>CC</sub> =5.0V; C <sub>L</sub> = 15pF	-	-	-	ns
			V <sub>CC</sub> =6.0V	-	-	39	ns
			LE̅ to Qn; see Figure 7	V <sub>CC</sub> =2.0V	-	-	215
		V <sub>CC</sub> =4.5V		-	-	43	ns
		V <sub>CC</sub> =5.0V; C <sub>L</sub> = 15pF		-	-	-	ns
		HIGH to LOW propagation delay	t <sub>PHL</sub>	MR̅ to Qn; see Figure 8	V <sub>CC</sub> =6.0V	-	-
V <sub>CC</sub> =2.0V	-				-	195	ns
V <sub>CC</sub> =4.5V	-				-	39	ns
V <sub>CC</sub> =5.0V; C <sub>L</sub> = 15pF	-				-	-	ns
transition time	t <sub>t</sub>	see Figure 7	V <sub>CC</sub> =6.0V	-	-	33	ns
			V <sub>CC</sub> =2.0V	-	-	95	ns
			V <sub>CC</sub> =4.5V	-	-	19	ns
pulse width	t <sub>w</sub>	LE̅ HIGH or LOW; see Figure 7	V <sub>CC</sub> =6.0V	-	-	16	ns
			V <sub>CC</sub> =2.0V	90	-	-	ns
			V <sub>CC</sub> =4.5V	18	-	-	ns
		MR̅ LOW; see Figure 8	V <sub>CC</sub> =6.0V	15	-	-	ns
			V <sub>CC</sub> =2.0V	90	-	-	ns
			V <sub>CC</sub> =4.5V	18	-	-	ns
set-up time	t <sub>su</sub>	D, An to LE; see Figure 9 and Figure 10	V <sub>CC</sub> =6.0V	-	-	-	ns
			V <sub>CC</sub> =2.0V	100	-	-	ns
			V <sub>CC</sub> =4.5V	20	-	-	ns
hold time	t <sub>h</sub>	D to LE; see Figure 9 and Figure 10	V <sub>CC</sub> =6.0V	-	-	-	ns
			V <sub>CC</sub> =2.0V	0	-	-	ns
			V <sub>CC</sub> =4.5V	0	-	-	ns
		An to LE; see Figure 9 and Figure 10	V <sub>CC</sub> =6.0V	0	-	-	ns
			V <sub>CC</sub> =2.0V	2	-	-	ns
			V <sub>CC</sub> =4.5V	2	-	-	ns
power dissipation capacitance	C <sub>PD</sub>	f <sub>i</sub> = 1MHz; V <sub>I</sub> =GND to V <sub>CC</sub>	V <sub>CC</sub> =6.0V	17	-	-	ns
			V <sub>CC</sub> =2.0V	2	-	-	ns
			V <sub>CC</sub> =4.5V	2	-	-	ns
<b>SN74HCT259</b>							
propagation delay	t <sub>pd</sub>	D to Qn; see Figure 5	V <sub>CC</sub> =4.5V	-	-	49	ns
			V <sub>CC</sub> =5.0V; C <sub>L</sub> = 15pF	-	-	-	ns
		An to Qn;	V <sub>CC</sub> =4.5V	-	-	51	ns

		see Figure 6	$V_{CC}=5.0V; C_L=15pF$	-	-	-	ns
		LE to Qn; see Figure 7	$V_{CC}=4.5V$	-	-	48	ns
			$V_{CC}=5.0V; C_L=15pF$	-	-	-	ns
HIGH to LOW propagation delay	$t_{PHL}$	$\overline{MR}$ to Qn; see Figure 8	$V_{CC}=4.5V$	-	-	49	ns
			$V_{CC}=5.0V; C_L=15pF$	-	-	-	ns
transition time	$t_t$	$V_{CC}=4.5V$ ; see Figure 7		-	-	19	ns
pulse width	$t_w$	LE HIGH or LOW; $V_{CC}=4.5V$ ; see Figure 7		24	-	-	ns
		MR LOW; $V_{CC}=4.5V$ ; see Figure 8		23	-	-	ns
set-up time	$t_{su}$	D, An to LE; $V_{CC}=4.5V$ ; see Figure 9 and Figure 10		21	-	-	ns
hold time	$t_h$	D to $\overline{LE}$ ; $V_{CC}=4.5V$ ; see Figure 9 and Figure 10		0	-	-	ns
		An to $\overline{LE}$ ; $V_{CC}=4.5V$ ; see Figure 9 and Figure 10		0	-	-	ns
power dissipation capacitance	$C_{PD}$	$f_i=1MHz; V_i=GND$ to $V_{CC}-1.5V$		-	-	-	pF

Note:

[ 1] Typical values are measured at nominal supply voltage ( $V_{CC}=3.3V$  and  $V_{CC}=5.0V$ ). [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in uW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$ =input frequency in MHz;

$f_o$ =output frequency in MHz;

$C_L$ =output load capacitance in pF;

$V_{CC}$ =supply voltage in V;

$N$ =number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

**AC Characteristics 3**

 ( $T_{amb} = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit			
<b>SN74HC259</b>									
propagation delay	$t_{pd}$	D to Qn; see Figure 5	$V_{CC}=2.0\text{V}$	-	-	280	ns		
			$V_{CC}=4.5\text{V}$	-	-	56	ns		
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	-	-	ns		
		An to Qn; see Figure 6	$V_{CC}=2.0\text{V}$	-	-	280	ns		
			$V_{CC}=4.5\text{V}$	-	-	56	ns		
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	-	-	ns		
			$V_{CC}=6.0\text{V}$	-	-	48	ns		
			$\overline{\text{LE}}$ to Qn; see Figure 7	$V_{CC}=2.0\text{V}$	-	-	255	ns	
				$V_{CC}=4.5\text{V}$	-	-	51	ns	
		$V_{CC}=5.0\text{V}; C_L=15\text{pF}$		-	-	-	ns		
		HIGH to LOW propagation delay	$t_{PHL}$	$\overline{\text{MR}}$ to Qn; see Figure 8	$V_{CC}=2.0\text{V}$	-	-	235	ns
					$V_{CC}=4.5\text{V}$	-	-	47	ns
$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-				-	-	ns		
$V_{CC}=6.0\text{V}$	-				-	40	ns		
transition time	$t_t$	see Figure 7	$V_{CC}=2.0\text{V}$	-	-	119	ns		
			$V_{CC}=4.5\text{V}$	-	-	22	ns		
			$V_{CC}=6.0\text{V}$	-	-	19	ns		
pulse width	$t_w$	$\overline{\text{LE}}$ HIGH or LOW; see Figure 7	$V_{CC}=2.0\text{V}$	105	-	-	ns		
			$V_{CC}=4.5\text{V}$	21	-	-	ns		
			$V_{CC}=6.0\text{V}$	18	-	-	ns		
		$\overline{\text{MR}}$ LOW; see Figure 8	$V_{CC}=2.0\text{V}$	105	-	-	ns		
			$V_{CC}=4.5\text{V}$	21	-	-	ns		
			$V_{CC}=6.0\text{V}$	18	-	-	ns		
set-up time	$t_{su}$	D, An to $\overline{\text{LE}}$ ; see Figure 9 and Figure 10	$V_{CC}=2.0\text{V}$	120	-	-	ns		
			$V_{CC}=4.5\text{V}$	24	-	-	ns		
			$V_{CC}=6.0\text{V}$	20	-	-	ns		
hold time	$t_h$	D to $\overline{\text{LE}}$ ; see Figure 9 and Figure 10	$V_{CC}=2.0\text{V}$	0	-	-	ns		
			$V_{CC}=4.5\text{V}$	0	-	-	ns		
			$V_{CC}=6.0\text{V}$	0	-	-	ns		
		An to $\overline{\text{LE}}$ ; see Figure 9 and Figure 10	$V_{CC}=2.0\text{V}$	2	-	-	ns		
			$V_{CC}=4.5\text{V}$	2	-	-	ns		
			$V_{CC}=6.0\text{V}$	2	-	-	ns		
power dissipation capacitance	$C_{PD}$	$f_i=1\text{MHz}; V_i=\text{GND to } V_{CC}$	-	-	-	pF			
<b>SN74HCT259</b>									
propagation delay	$t_{pd}$	D to Qn; see Figure 5	$V_{CC}=4.5\text{V}$	-	-	59	ns		
			$V_{CC}=5.0\text{V}; C_L=15\text{pF}$	-	-	-	ns		
		An to Qn;	$V_{CC}=4.5\text{V}$	-	-	62	ns		

		see Figure 6	$V_{CC}=5.0V; C_L=15pF$	-	-	-	ns
		LE to Qn; see Figure 7	$V_{CC}=4.5V$	-	-	57	ns
			$V_{CC}=5.0V; C_L=15pF$	-	-	-	ns
HIGH to LOW propagation delay	$t_{PHL}$	MR to Qn; see Figure 8	$V_{CC}=4.5V$	-	-	59	ns
			$V_{CC}=5.0V; C_L=15pF$	-	-	-	ns
transition time	$t_t$	$V_{CC}=4.5V$ ; see Figure 7		-	-	22	ns
pulse width	$t_w$	LE HIGH or LOW; $V_{CC}=4.5V$ ; see Figure 7		29	-	-	ns
		MR LOW; $V_{CC}=4.5V$ ; see Figure 8		27	-	-	ns
set-up time	$t_{su}$	D, An to LE; $V_{CC}=4.5V$ ; see Figure 9 and Figure 10		26	-	-	ns
hold time	$t_h$	D to LE; $V_{CC}=4.5V$ ; see Figure 9 and Figure 10		0	-	-	ns
		An to LE; $V_{CC}=4.5V$ ; see Figure 9 and Figure 10		0	-	-	ns
power dissipation capacitance	$C_{PD}$	$f_i=1MHz; V_i=GND$ to $V_{CC}-1.5V$		-	-	-	pF

**Note:**

[ 1] Typical values are measured at nominal supply voltage ( $V_{CC}=3.3V$  and  $V_{CC}=5.0V$ ). [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in uW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$ =input frequency in MHz;

$f_o$ =output frequency in MHz;

$C_L$ =output load capacitance in pF;

$V_{CC}$ =supply voltage in V;

$N$ =number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ =sum of outputs.

## Testing Circuit

### AC Testing Circuit

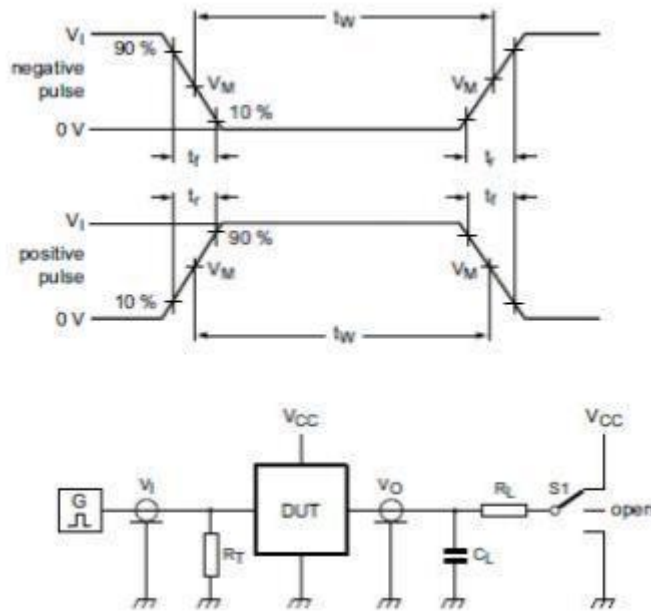


Figure 4. Test circuit for measuring switching times

Definitions for test circuit:

$C_L$ =Load capacitance including jig and probe capacitance.

$R_T$ =Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$R_L$ =Load resistance.

S1=Test selection switch.

### AC Testing Waveforms

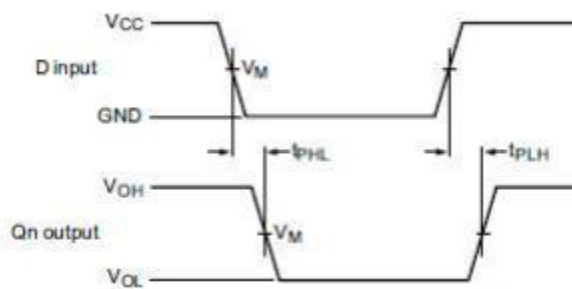


Figure 5. Data input to output propagation delays

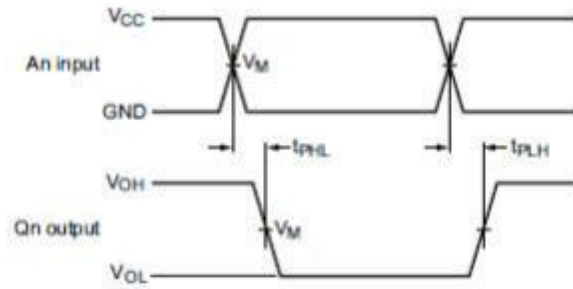


Figure 6. Address input to output propagation delays

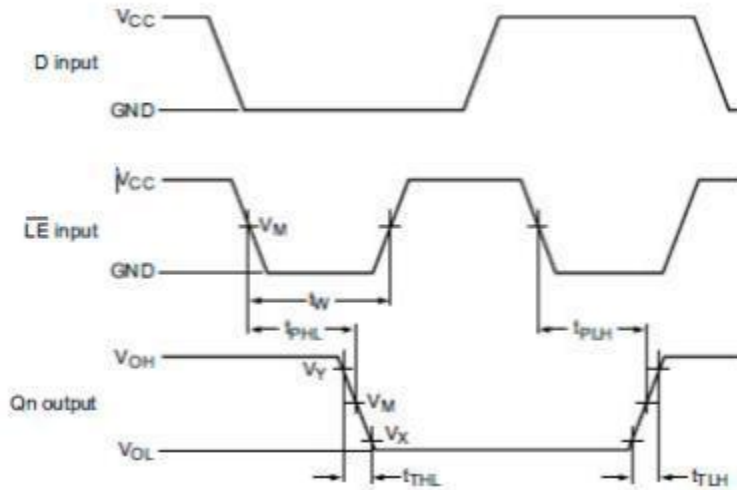


Figure 7. Enable input to output propagation delays and pulse width

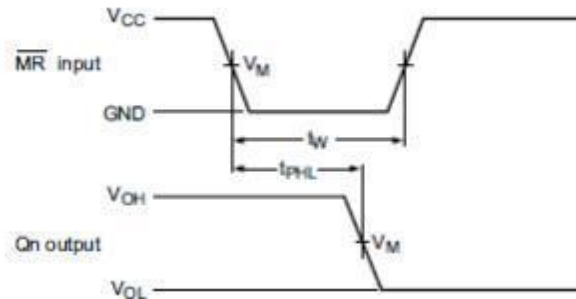


Figure 8. Master reset input to output propagation delay

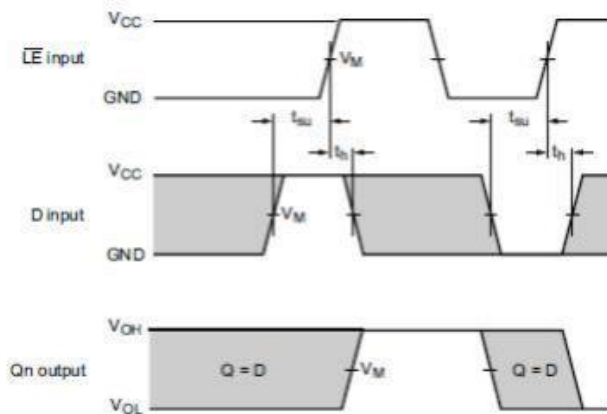


Figure 9. Data input to latch enable input set-up and hold times

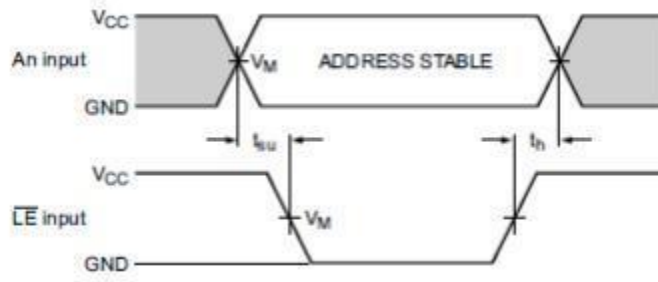


Figure 10. Address input to latch enable input set-up and hold times

**Measurement Points**

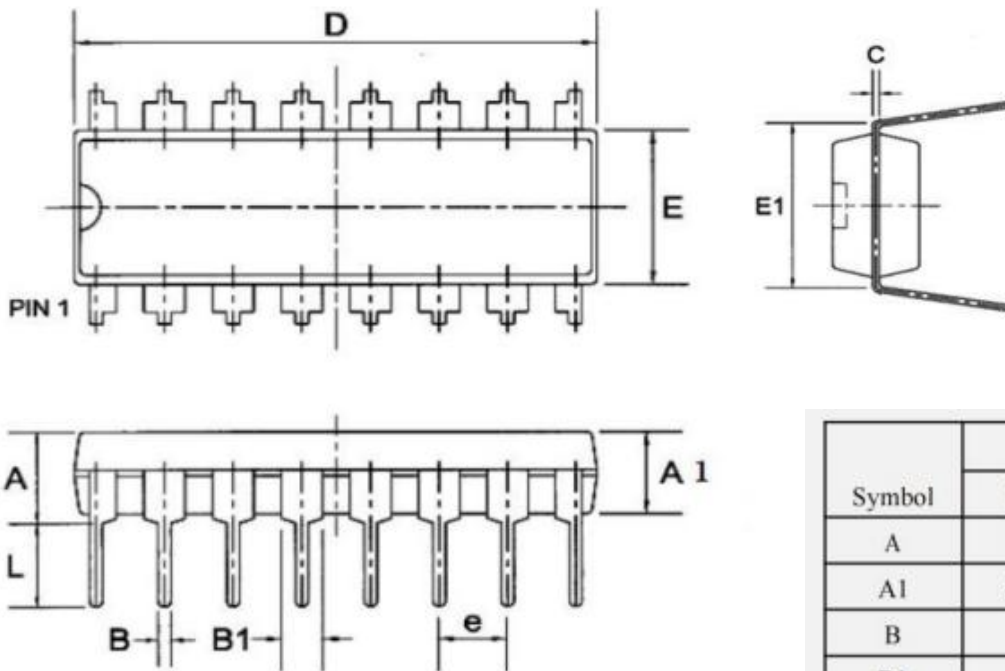
Type	Input		Output	
	$V_M$	$V_M$	$V_X$	$V_Y$
SN74HC259	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$
SN74HCT259	1.3V	1.3V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$

**Test Data**

Type	Input		Load		S1 position
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
SN74HC259	$V_{CC}$	6ns	15pF, 50pF	1k $\Omega$	open
SN74HCT259	3V	6ns	15pF, 50pF	1k $\Omega$	open

**Package Information**

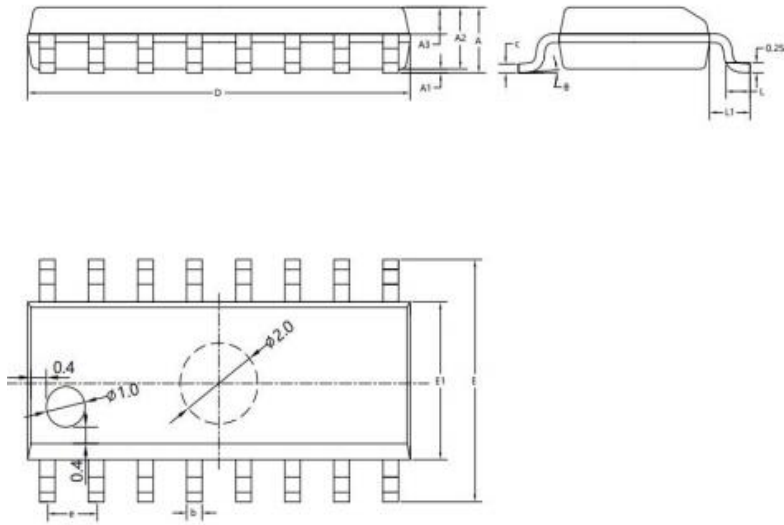
DIP16



Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A	--	--	4.31
A1	3.15	3.30	3.65
B	--	0.50	--
B1	--	1.6	--
C	--	0.27	--
D	19.00	19.20	19.60
E	6.20	6.50	6.60
E1	--	8.0	--
e	--	2.3	--
L	3.00	3.20	3.60

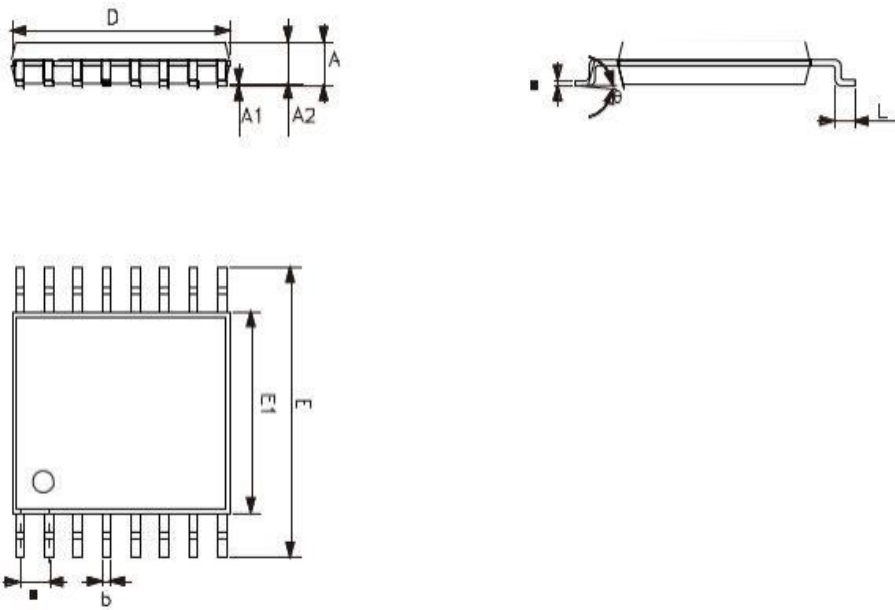


SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
Ø	0"	4"	8"

TSSOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
9	0.	8.