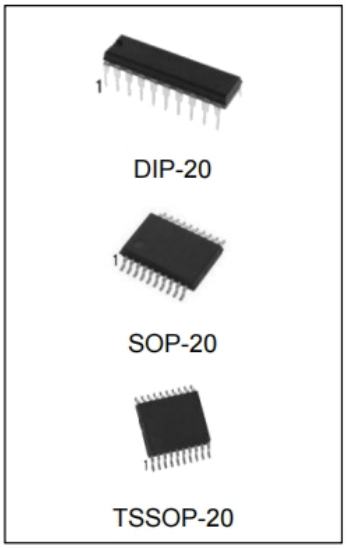
General Description

The 74HC534 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops. The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs.When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops



Features

- Input levels: CMOS level
- 3-state inverting outputs for bus oriented applications
- 8-bit positive,edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Specified from -40℃ to +105℃
- Packaging information:DIP-20/SOP-20/TSSOP-20

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
74HC534N	DIP-20	74HC534	TUBE	720pcs/box
74HC534M/TR	SOP-20	74HC534	REEL	2000pcs/reel
74HC534MT/TR	TSSOP-20	HC534	REEL	2500pcs/reel

Block Diagram

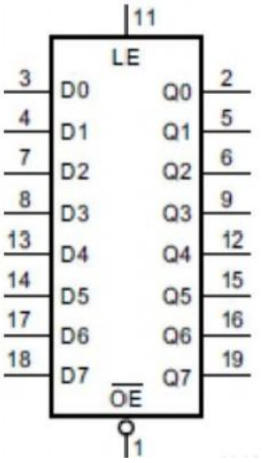


Figure 1.Logic symbol

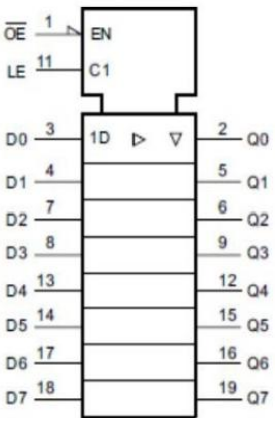


Figure 2.IEC logic symbol

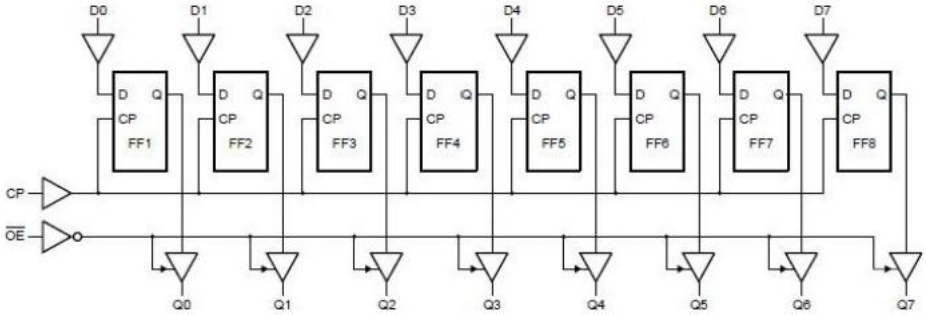


Figure 3.Logic diagram

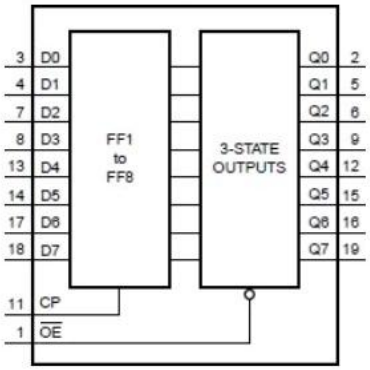
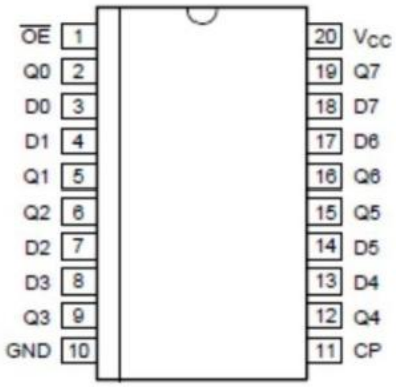


Figure 4.Functional diagram

Pin Configurations



DIP-20/SOP-20/TSSOP-20

Pin Description

Pin No.	Pin Name	Description
1	OE	output enable input (active LOW)
2	Q0	data output
3	D0	data input
4	D1	data input
5	Q1	data output
6	Q2	data output
7	D2	data input
8	D3	data input
9	Q3	data output
10	GND	ground (0V)
11	CP	clock input (LOW-to-HIGH,edge-triggered)
12	Q4	data output
13	D4	data input
14	D5	data input
15	Q5	data output
16	Q6	data output
17	D6	data input
18	D7	data input
19	Q7	data output
20	Vcc	supply voltage

Function Table

Operating modes	Input			Internal flip-flops	Output
	OE	CP	Dn		Qn
Load and read register	L	↑		L	L
	L	↑	h	H	H
Load register and disable outputs	H			L	Z
	H	↑	h	H	Z

Note:H=HIGH voltage level;L=LOW voltage level;X=don't care;Z=high-impedance OFF-state;
h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑=LOW-to-HIGH clock transition.

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to GND(ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Max	Unit
supply voltage	VCC			-0.5	+7.0	V
input clampingcurrent	IIK	Vi<-0.5V or V_1>Vcc+0.5V			±20	mA
output clampingcurrent	IOK	Vo<-0.5V or Vo>Vcc+0.5V			±20	mA
output current	Io	-0.5V<Vo<Vcc+0.5V			±35	mA
supply current	Icc				70	mA
ground cumen	IGND			-70		mA
storage temperature	Tstg			-65	+150	℃
total powerdissipation	Ptot				500	mW
Soldering temperature	TL	10s	DIP	245		℃
			SOP	245		

Note:1、Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.Operating Ratings indicate conditions for which the device is intended to be functional,but specific performance is not ensured.

2、For DIP20 packages:above 70℃ the value of Pot derates linearly with 12mW/K.

3、For SOP20 packages:above 70℃ the value of Put derates linearly with 8mWIK.

4、ForTSSOP20 packages:above 60℃ the value of Put derates linearly with 5.5mW/K.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max.	Unit
supply voltage	Vcc		2.0	5.0	6.0	V
input voltage	Vi		0	—	Vcc	V
output voltage	Vo		0		Vcc	V
nput transition rise and fall rate	ΔtΔV	Vcc=2.0V			625	nsN
		Vcc=4.5V		1.67	139	nsN
		Vcc=6.0V		—	83	nsN
ambient temperature	Tamb		-40		+105	℃

Electrical Characteristics

DC Characteristics 1

(Tamb=25℃,voltages are referenced to GND(ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH-level input voltage	VH	Vcc=2.0V		1.5	1.2		V
		Vcc=4.5V		3.15	2.4		V
		Vcc=6.0V		4.2	3.2		V
LOW-level input voltage	VL	Vcc=2.0V			0.8	0.5	V
		Vcc=4.5V			2.1	1.35	V
		Vcc=6.0V			2.8	1.8	V
HIGH-level output voltage	Voh	Vi=Vh or VL	Io=-20uA;Vcc=2.0V	1.9	2.0		V
			Io=-20uA;Vcc=4.5V	4.4	4.5		V
			Io=-20uA;Vcc=6.0V	5.9	6.0		V
			o=-6.0mA;Vcc=4.5V	3.98	4.32		V
			o=-7.8mA;Vcc=6.0V	5.48	5.81		V
LOWHevel outpuf voltage	Vol	Vi=VH or VL	Io=20uA;Vcc=2.0V		0	0.1	V
			Io=20uA;Vcc=4.5V		0	0.1	V
			Io=20uA;Vcc=6.0V		0	0.1	V
			Io=6.0mA;Vcc=4.5V		0.15	0.26	V
			Io=7.8mA;Vcc=6.0V		0.16	0.26	V
input leakage current	I	Vi=Vcc or GND;Vcc=6.0V				±0.1	uA
OFF-state output current	loz	Vi=Vh or VL;Vcc=6.0V; Vo=Vcc or GND				±0.5	uA
supply current	Icc	Vi=Vcc or GND;Io=0A;Vcc=6.0V				8.0	uA
input capacitance	Ci				3.5		pF

DC Characteristics 2

(Tamb=-40℃ to +85℃, voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
HIGH-level input voltage	ViH	Vcc=2.0V		1.5			V
		Vcc=4.5V		3.15			V
		Vcc=6.0V		**4.2**			V
LOW-level input voltage	VL	Vcc=2.0V				0.5	V
		Vcc=4.5V				1.35	V
		Vcc=6.0V				1.8	V
HIGH-level output voltage	VoH	V_1=Vh or VL	Io=-20uA;Vcc=2.0V	1.9			V
			Io=-20uA;Vcc=4.5V	4.4			V
			Io=-20uA;Vcc=6.0V	5.9			V
			Io=-6.0mA;Vcc=4.5V	3.84			V
			Io=-7.8mA;Vcc=6.0V	5.34			V
LOW-level output voltage	Vol	V_1=Vh or VL	Io=20uA;Vcc=2.0V			0.1	V
			Io=20uA;Vcc=4.5V			0.1	V
			Io=20uA;Vcc=6.0V			0.1	V
			Io=6.0mA;Vcc=4.5V			0.33	V
			Io=7.8mA;Vcc=6.0V			0.33	V
nput leakage current	I	V=Vcc or GND;Vcc=6.0V		—		±1.0	uA
OFF-state output current	loz	Vi=Vih or VL;Vcc=6.0V Vo=Vcc or GND				±5.0	uA
supply current	Icc	V=Vcc or GND;Io=0A;Vcc=6.0V				80	uA

DC Characteristics 3

(Tamb=40℃ to +105℃,voltages are referenced to GND(ground=0V),unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max	Unit
HIGH-level inpu voltage	VH	Vcc=2.0V		1.5			V
		Vcc=4.5V		3.15			V
		Vcc=6.0V		4.2			V
LOW-level input voltage	VL	Vcc=2.0V				0.5	V
		Vcc=4.5V				1.35	V
		Vcc=6.0V				1.8	V
HIGH-level output voltage	VoH	V_1=Vih or VL	Io=-20uA;Vcc=2.0V	1.9			V
			Io=-20uA;Vcc=4.5V	4.4			V
			Io=-20uA;Vcc=6.0V	5.9			V
			Io=-6.0mA;Vcc=4.5V	3.7			V
			o=-7.8mA;Vcc=6.0V	5.2			V
LOW-level output voltage	Vou	V_1=Vih or VL	Io=20uA;Vcc=2.0V			0.1	V
			Io=20uA;Vcc=4.5V			0.1	V
			Io=20uA;Vcc=6.0V			0.1	V
			Io=6.0mA;Vcc=4.5V			0.4	V
			Io=7.8mA;Vcc=6.0V			0.4	V
nput leakage current	I	V=Vcc or GND;Vcc=6.0V				±1.0	uA
OFF-state output current	loz	Vi=Vih or VL;Vcc=6.0V; Vo=Vcc or GND				±10	uA
supply curren	Icc	V=Vcc or GND;Io=0A;Vcc=6.0V		—		160	uA

AC Characteristics 1

(Tamb=25℃,GND=0V,CL=50pF,unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CP to Qn propagation delay	tpd	see Figure 6	Vcc=2.0V		41	165	ns
			Vcc=4.5V		15	33	NS
			Vcc=5.0V;CL=15pF		12		ns
			Vcc=6.0V	—	12	28	NS
OE to Qn enable time	ten	see Figure g	Vcc=2.0V		33	150	nS
			Vcc=4.5V	—	12	30	NS
			Vcc=6.0V		10	26	ns
OE to Qn disable time	tdis	see Figure 8	Vcc=2.0V		41	150	ns
			Vcc=4.5V		15	30	NS
			Vcc=6.0V		12	26	ns
transition time	tt	Qn output;see Figure 6	Vcc=2.0V		14	60	ns
			Vcc=4.5V		5	12	ns
			Vcc=6.0V	—	4	10	NS
pulse width	tw	CP;HIGH or LOW see Figure 6	Vcc=2.0V	80	19		ns
			Vcc=4.5V	16	7		NS
			Vcc=6.0V	14	5		ns
Dn to CP set-up time	tsu	see Figure 7	Vcc=2.0V	60	6		ns
			Vcc=4.5V	12	2		NS
			Vcc=6.0V	10	2		NS
Dn to CP hold time	th	see Figure 7	Vcc=2.0V	5	-3		ns
			Vcc=4.5V	5	-1		ns
			Vcc=6.0V	5	-1		NS
maximum frequency	fmax	CP input;see Figure 6	Vcc=2.0V	6.0	18		MHz
			Vcc=4.5V	30	55		MHz
			Vcc=5.0V;CL=15pF		61		MHz
			Vcc=6.0V	35	66		MHz
power dissipation capacitance	CPD	Vi=GND to Vcc			19		pF

Note:
(1)tpa is the same as tpuhand tpHl.
(2) ten is the same as tpzt and tpzH.
(3) ttis is the same as tpuz and tpHz.
(4) t is the same as trhland truh.
(5)Cpp is used to determine the dynamic power dissipation (Pp in uW).
$P_o=C_{pp}\times V_{cc}^2\times f_1+Z(C_l\times V_{cc}^2\times f_o)$ where:
f=input frequency in MHz;f_o=output frequency in MHz;
CL=output load capacitance in pF;
Vcc=supply voltage in V;
$Z(C_L\times V_{cc}^2\times f_o)$=sum of outputs.

AC Characteristics 2

Tamb=-40℃ to +85℃,GND =0V,CL=50pF,unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ	Max.	Unit
CP to Qn propagation delay	tpa	see Figure 6	Vcc=2.0V			205	NS
			Vcc=4.5V			41	ns
			Vcc=6.0V			35	NS
OE to Qn enable time	ten	see Figure 8	Vcc=2.0V			190	NS
			Vcc=4.5V			38	NS
			Vcc=6.0V			33	NS
OE to Qn disable time	tdis	see Figure g	Vcc=2.0V			190	ns
			Vcc=4.5V			38	NS
			Vcc=6.0V			33	NS
transition time	tt	Qn output;see Figure 6	Vcc=2.0V			75	NS
			Vcc=4.5V			15	ns
			Vcc=6.0V			13	ns
pulse width	tw	CP;HIGH or LOW; see Figure 6	Vcc=2.0V	100			NS
			Vcc=4.5V	20			NS
			Vcc=6.0V	17			ns
Dn to CP set-up time	tsu	see Figure 7	Vcc=2.0V	75			NS
			Vcc=4.5V	15			NS
			Vcc=6.0V	13			NS
Dn to CP hold time	th	see Figure 7	Vcc=2.0V	5			NS
			Vcc=4.5V	5			NS
			Vcc=6.0V	5			NS
maximum frequency	fmax	CP input;see Figure 6	Vcc=2.0V	4.8			MHz
			Vcc=4.5V	24			MHz
			Vcc=6.0V	28			MHz

Note:

(1) toa is the same as trLh and tpHL.

(2) ten is the same as trzt and tpzH.

(3) tais is the same as tpuz and tpHz.

(4) t is the same as trHr and truh.

AC Characteristics 3

(Tamb=-40℃ to+105℃,GND=0V,CL=50pF,unless otherwise specified.)

Parameter	Symbol	Conditions		Min	Typ.	Max.	Unit
CP to Qn propagatior delay	tpd	see Figure G	Vcc=2.0V			250	NS
			Vcc=4.5V			50	ns
			Vcc=6.0V			43	NS
OE to Qn enable time	ten	see Figure &	Vcc=2.0V			225	NS
			Vcc=4.5v			45	ns
			Vcc=6.0V			38	ns
OEto Qn disable time	tis	see Figure 8	Vcc=2.0V			225	ns
			Vcc=4.5V			45	NS
			Vcc=6.0V			38	ns
transition time	tt	Qn output;see Figure 6	Vcc=2.0v			90	NS
			Vcc=4.5V			18	ns
			Vcc=6.0V			15	NS
pulse width	tw	CP;HIGH or LOW; see Figure 6	Vcc=2.0V	120			NS
			Vcc=4.5V	24			NS
			Vcc=6.0V	20			NS
Dn to CP set-up time	tsu	see Figure 7	Vcc=2.0V	90			NS
			Vcc=4.5V	18			NS
			Vcc=6.0V	15			ns
Dn to CP hold time	tn	see Figure 7	Vcc=2.0V	5			NS
			Vcc=4.5V	5			NS
			Vcc=6.0V	5			NS
maximum frequency	fmax	CP input;see Figure 6	Vcc=2.0V	4.0			MHz
			Vcc=4.5v	20			MHz
			Vcc=6.0V	24			MHz

Note:

(1) tpa is the same as trLH and tpHL.

(2) ten is the same as tpz and tpzh.

(3) tais is the same as tpuz and tpHz.

(4) t is the same as trHl and truh.

Testing Circuit

AC Testing Circuit

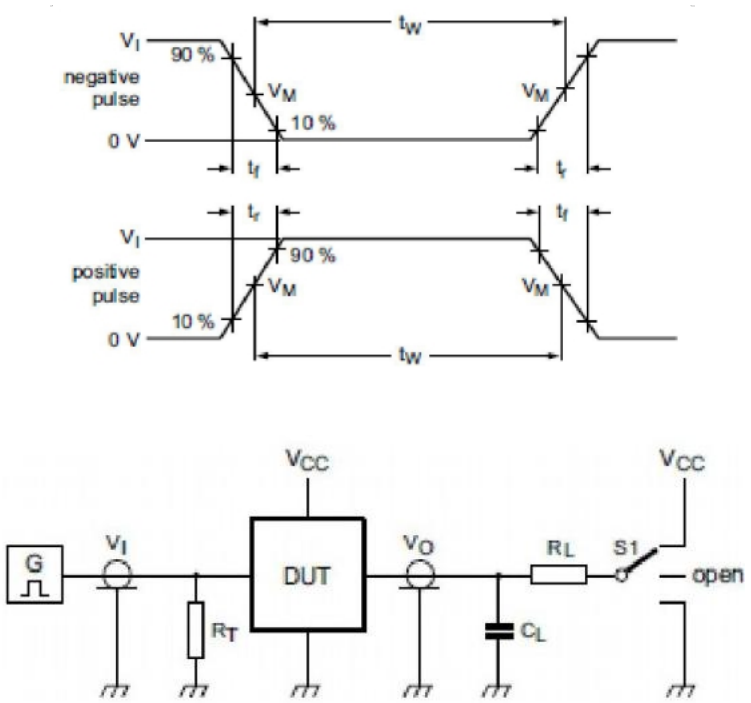


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

RL=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z° of the pulse generator.

S1=Test selection switch.

AC Testing Waveforms

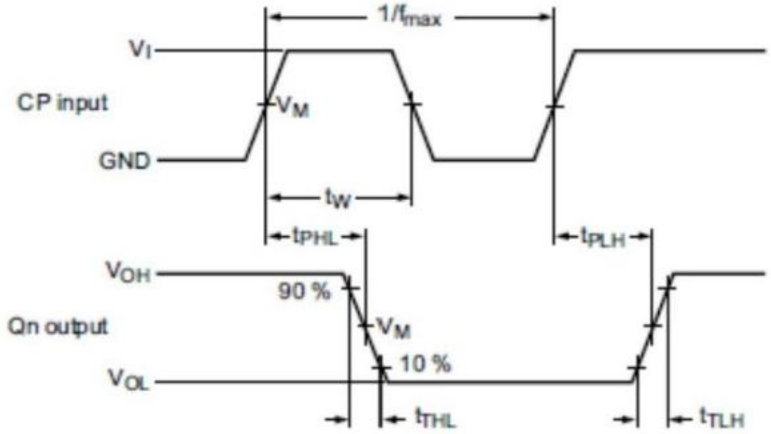


Figure 6. Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)

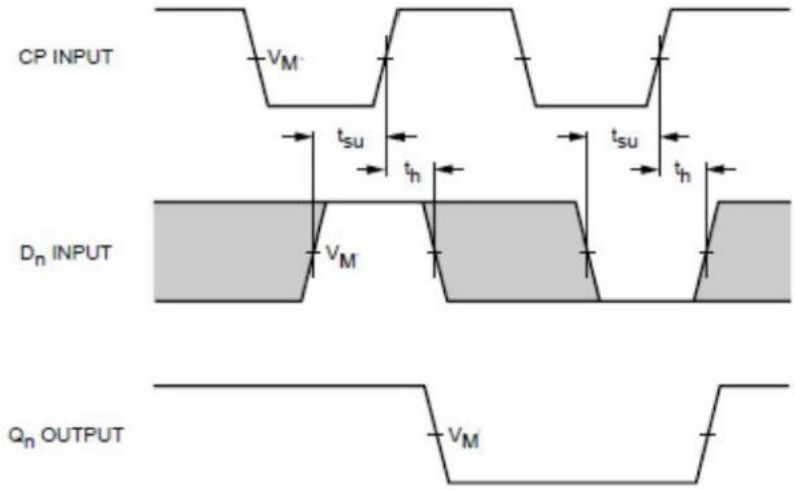


Figure 7. The data input (D) to clock input (CP) set-up times and clock input (CP) to data input (D) hold times

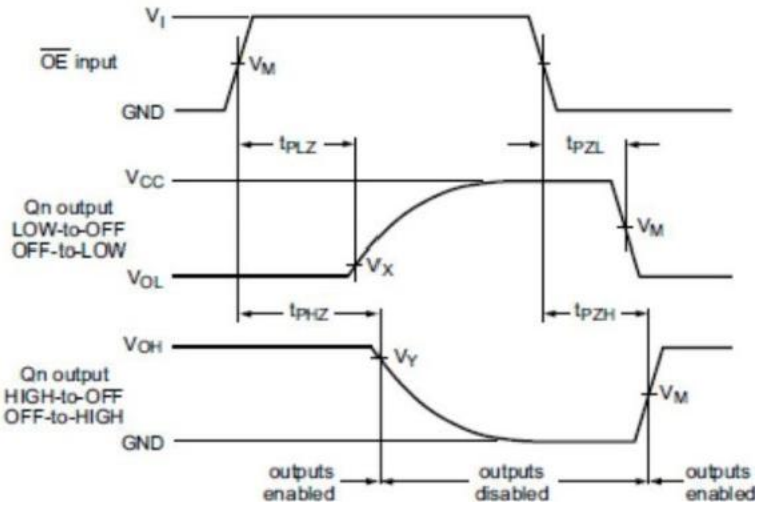


Figure 8.Enable and disable times

Measurement Points

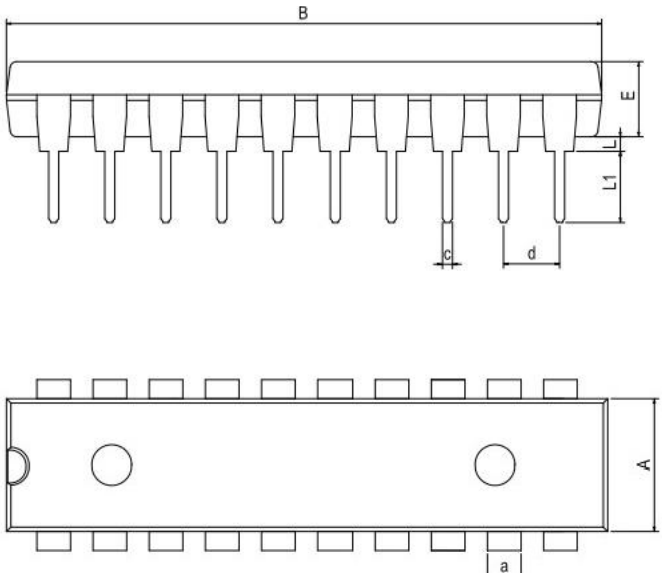
Type	Input	Output		
	VM	Vm	Vx	Vy
74HC534	**0.5×Vcc**	0.5×Vcc	0.1×Vcc	0.9×Vcc

Test Data

Type	Input		Load		S1 position		
	V_1	tr,tf	CL	RL	tpHL tpLH	tpzH tpHz	[PZL, tpLz
74HC534	Vcc	**6ns**	15pF,50pF	**1kΩ**	**open**	**GND**	Vcc

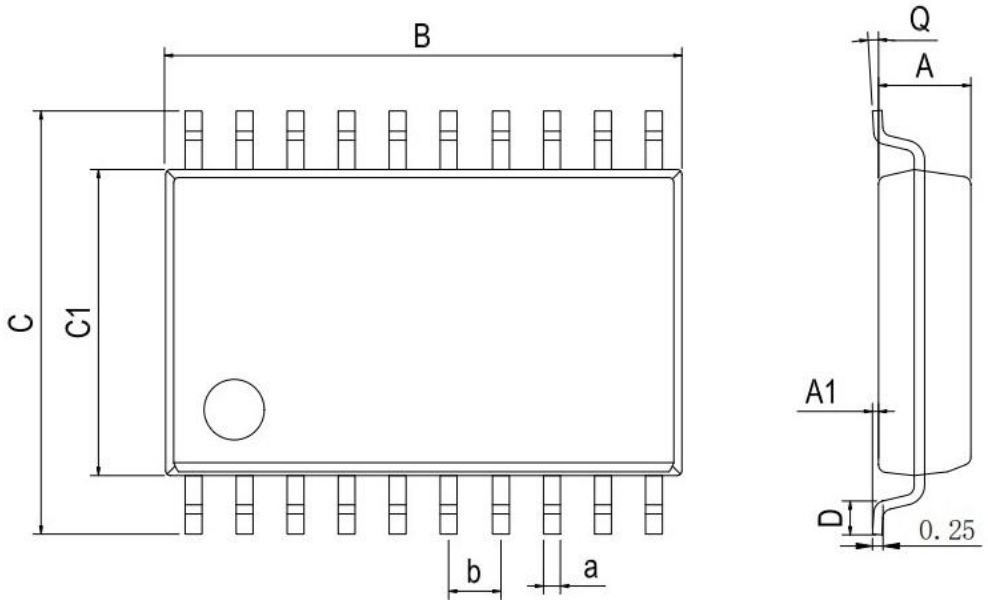
Physical Dimensions

DIP-20



Dimensions In Millimeters(DIP-20)										
Symbol:	A	B	D	D1	E	L	**L1**	**a**	**C**	**d**
Min:	6.10	24.95	8.10	7.42	3.10	0.50	**3.00**	**1.50**	**0.40**	**2.54 BSC**
Max:	6.68	26.55	10.9	7.82	3.55	0.70	**3.60**	**1.55**	**0.50**	

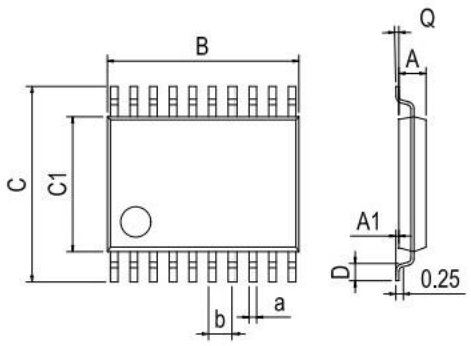
SOP-20



Dimensions In Millimeters(SOP-20)									
Symbol:	**A**	**A1**	B	C	**C1**	**D**	**Q**	**a**	**b**
Min:	2.10	0.05	12.50	10.21	**7.40**	**0.45**	**0°**	**0.35**	**1.27 BSC**
Max:	2.50	0.25	13.00	10.61	**7.60**	**1.25**	**8°**	**0.45**	

Physical Dimensions

TSSOP-20



Dimensions In Millimeters(TSSOP-20)									
Symbol:	**A**	**A1**	**B**	C	C1	**D**	**Q**	**a**	**b**
Min:	0.85	0.05	6.40	6.20	4.30	**0.40**	**0°**	**0.20**	**0.65 BSC**
Max:	1.05	0.20	6.60	6.60	**4.50**	**0.80**	**8°**	**0.25**	