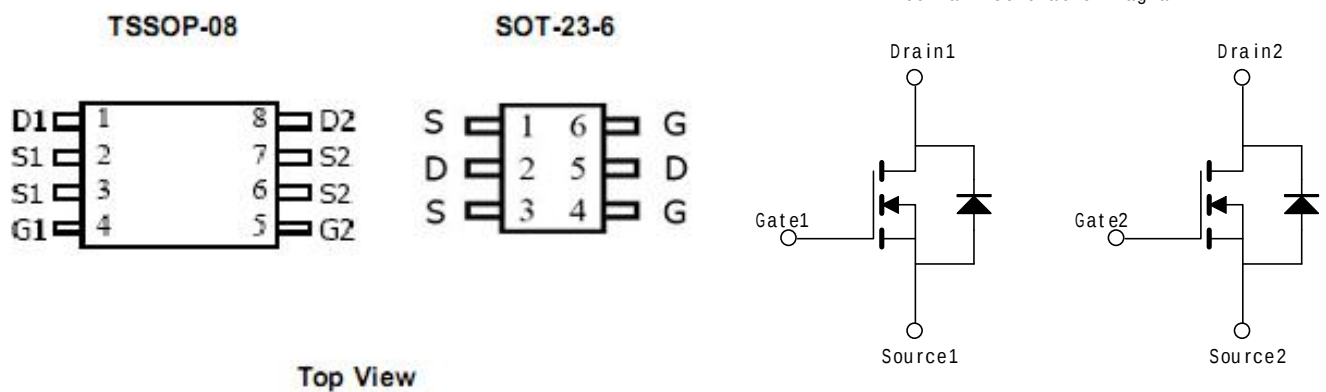


1. Features

- n** $R_{DS(ON)}$, $V_{GS}@1.8V$, $I_{DS}@2.0A = 75m\Omega$
- n** $R_{DS(ON)}$, $V_{GS}@2.5V$, $I_{DS}@3.5A = 38m\Omega$
- n** $R_{DS(ON)}$, $V_{GS}@4.0V$, $I_{DS}@4.5A = 30m\Omega$
- n** $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_{DS}@4.5A = 28m\Omega$
- n** $R_{DS(ON)}$, $V_{GS}@10V$, $I_{DS}@5.0A = 25m\Omega$
- n** Advanced trench process technology
- n** High Density Cell Design For Ultra Low On-Resistance
- n** High Power and Current handing capability
- n** Ideal for Li ion battery pack applications

2. Pin information



3. Maximum Ratings and Thermal Characteristics

($T_A = 25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current ¹		I_D	5	A
Pulsed Drain Current ²		I_{DM}	20	
Maximum Power Dissipation	$T_A = 25^\circ C$	P_D	2	W
	$T_A = 75^\circ C$		1.28	
Operating Junction and Storage Temperature Range		T_{J1} T_{stg}	-55 to 150	$^\circ C$
Junction-to-Ambient Thermal Resistance (PCB mounted) ³		$R_{\theta JA}$	62.5	$^\circ C/W$

Note: 1. Fused current that based on wire numbers and diameter

2. Repetitive Rating: Pulse width limited by the maximum junction temperature

3. 1-in² 2oz Cu PCB board

4. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V,I _D = 250uA	20			V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 1.8V,I _D = 2.0A		53.0	75.0	mΩ
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 2.5V,I _D = 3.5A		30.0	38.0	
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 4.0V,I _D = 4.5A		23.0	30.0	
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 4.5V,I _D = 4.5A		22.0	28.0	
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V,I _D = 5.0A		20.0	25.0	
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{GS} ,I _D = 250uA	0.5	0.75	1	V
Zero Gate Voltage drain Current	I _{DSS}	V _{GS} = 20V,V _{GS} = 0V			1	uA
Gate Body Leakage	I _{GSS}	V _{GS} = ±12V,V _{DS} = 0V			±100	nA
Dynamic ³						
Total Gate Charge	Q _G	V _{DS} = 10V,I _D = 6A V _{GS} = 4.5V		6.24	8.11	nC
Gate-Source Charge	Q _{GS}			1.64	2.13	
Gate-Drain Charge	Q _{GB}			1.34	1.74	
Tum-On Delay Time	T _{d(on)}	V _{DD} = 10V,I _D = 6A I _D = 1A,V _{GS} = 4.5V		10.4	20.8	ns
Tum-On Rise Time	T _r			4.4	8.8	
Tum-Off Delay Time	T _{d(off)}			27.36	54.72	
Tum-Off Fall Time	T _f			4.16	8.32	
Input Capacitance	C _{iss}	V _{DS} = 8V,V _{GS} = 0V f =1.0MHz		522.3		pF
Output Capacitance	C _{Oss}			98.48		
Reverse Transfer Capacitance	C _{rss}			74.69		
Source-Drain Diode						
Max.Diode Forward Current	I _S				1.7	A
Diode Forward Voltage	V _{SD}	I _S = 1.7A,V _{GS} = 0V		0.74		V

Note: Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%

3. Guaranteed by design; not subject to production testing

5. Typical Characteristics Curves ($T_a=25^{\circ}\text{C}$, unless otherwise note)

