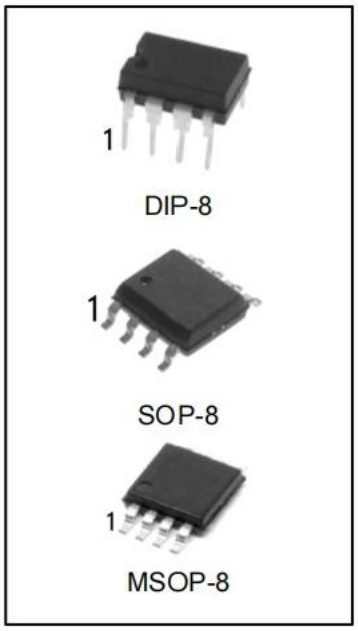
General Description

The HG93Cxx family provides 1K,2K and 4K of serial electrically erasable and programmable read-only memory (EEPROM).The wide Vdd range allows for low-voltage operation down to 1.8V and up to 5.5V.The device,fabricated using traditional CMOS EEPROM technology,is optimized for many ndustrial and commercial applications where low-voltage and low-power operation is essential.The 93C46/56/66 is available in 8-pin DIP,8-pin JEDEC SOP,and 8-pin MSOP packages and is accessed via a 3-wire serial interface

Features

- Internally organized as 128x8 or64x16(1K),256x8 or 128x16 (2K) 512x8or 256x16(4K)
- Wide-voltage range operation 1.8V-5.5 V
- 3-wire serial interface bus
- Data retention:100 years
- High endurance:1,000,000 Write Cycles
- 2 MHz(5V)clock rate
- Sequential read operation
- Self-timed write cycle (10ms max)
- 8-pin DIP,8-pin JEDEC SOP,and 8-pin MSOP Packages

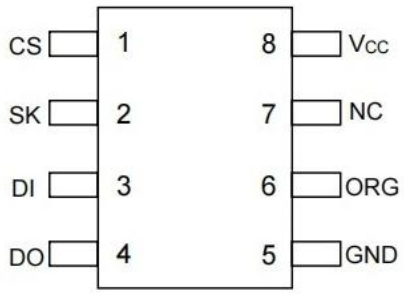


Order Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
93C46N	DIP-8	93C46	TUBE	2000/box
93C56N	DIP-8	93C56	TUBE	2000/box
93C66N	DIP-8	93C66	TUBE	2000/box
93C46M/TR	SOP-8	93C46	REEL	2500/reel
93C56M/TR	SOP-8	93C56	REEL	2500/reel
93C66M/TR	SOP-8	93C66	REEL	2500/reel
93C46MM/TR	MSOP-8	93C46	REEL	3000/reel
93C56MM/TR	MSOP-8	93C56	REEL	3000/ree
93C66MM/TR	MSOP-8	93C66	REEL	3000/reel

Figure 1.Pin Configurations

8-pin DIP/MSOP/SOP



Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
NC	No Connect

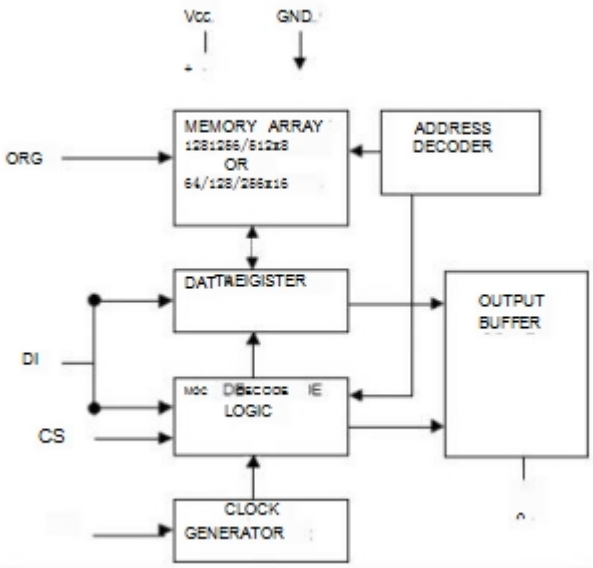
ABSOLUTE MAXIMUM RATINGS

Symbo	Parameter	Value	Unit
Tstg	Storage Temperature	-65to150	℃
Twk	Operating Temperature	-40to+85	℃
TL	Lead Temperature(Soldering,10 seconds)	245	℃
Voltage on Any Pin with			
Vcc	Respect to Ground	7.0	V
Vcc	Maximum Operating Voltage	6.25	V
Io	DC Output Current	5.0	mA

Note:Stresses beyond those listed under “Absolute Maximum Ratings”may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2.Block Diagram



Notes

1.The ORG pin is used to select between x8 and x16 mode.When the pin is connected to Vcc, x16.mode is selected.Otherwise,the ORG pin should be grounded in order to select x8 mode.

The interface for the HG93C46156166 is accessed through four different signals:

Chip Select (CS),Data Input (DI),Data Output (DO),and Serial Data Clock (SK).The Chip Select (CS) signal must be pulled high before issuing a command through the Data Input (DI)pin.The Serial Data Clock (SK)signal is used in conjunction with the Data Input (DI)pin.

PIN CAPACITANCE

Applicable over recommended operating range from TA=25° ℃, f=1.0 MHz, Vcc=+5.0V

Symbol	Test Condition	Max	Units	Conditior
Cout	Output Capacitance (DO)	5	pF	Vour=0V
CIN	Input Capacitance (CK,SK,DI)	5	pF	Vin=0V

Note:1.This parameter is characterized and not 100%tested.

DC CHARACTERISTICS

Applicable over recommended operating range from:

TAMB=-40° Cto+85° C, Vcc=+1.8V to+5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Vcc1	Supply Voltage		1.8		5.5	V
Vcc2	Supply Voltage		2.7		5.5	V
Vcc?	Supply Voltage		4.5		5.5	V
Icc	Supply Current Vcc5.0V	READ at MHz		0.5	2.0	μA
Icc	Supply Current Vcc5.0V	WRITE at 1MHz		0.5	2.0	μA
IsB1	Supply Current Vcc1.8V	CS=0V		0	0.1	μA
IsB2	Supply Current Vcc2.7V	CS=0V		6.0	10.0	μA
IsB3	Supply Current Vcc5.0V	CS=0V		17	30	μA
Iu	Input Leakage Current	Vin=OV to Vcc		0.1	3.0	μA
Ilo	Output Leakage Current	Vin=OV to Vcc		0.1	3.0	μA
VL1(VHYY	Input Low Level Input High Leve	2.7V<Vcc<5.5V	-0.6 2.0		0.8 Vcc+1	V
VL21 ViH2(1	Input Low Level Input High Level	1.8V<Vcc<2.7V	-0.6 Vcc×0.7		Vcc×0.3 Vcc+1	V
VoL1 VoH1	Output Low Level Output High Level	2.7V<Vcc<5.5V;Ior=2.1mA Ioh=-0.4mA	2.4		0.4	V
VoL_2 VoHz	Output Low Level Output High Level	1.8V<Vcc <2.7V;Iol=0.15mA Ioh=-100uA	Vcc-0.2		0.2	V

Note:1.Vu and Vin max are reference only and are not tested

AC CHARACTERISTICS

Applicable over recommended operating range from:

TAMB=-40℃ to+85° ℃, Vcc=As specified, CL=1 TTL Gate &100pF (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
fsk	Clock Freguency SK	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V		0 0 0		 0.25	MHZ
tskh	SK High Time	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V		250 250 1000			NS
tskl	SK Low Time	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V		250 250 1000			NS
tcs	Minimum CS Low Time	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V		250 250 1000			ns
tcss	CS Setup Time	Relative to SK	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V	50 50 200			ns
tois	DI Setup Time	Relative to SK	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V	100 100 400			ns
tcsh	CS Hold Time	Relative to SK		0			ns
toiH	DI Hold Time	Relative to SK	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V	100 100 400			NS
tpD1	Output Delay tc “1”	AC Test	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V			250 250 1000	ns
tPDo	Output Delay to “0”	AC Test	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V			250 250 1000	ns
tsv	CS to Status Valid	AC Test	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V			250 250 1000	NS
toF	CS to DO in High Impedance	AC TestCS =VL	4.5V<Vcc<5.5V 2.7V<Vcc<5.5V 1.8V<Vcc<5.5V			100 100 400	ns
twp	Write Cycle Time		4.5V<Vcc<5.5V		3	10	ms
Endurance	5.0V,25℃			1M			Write Cycles

INSTRUCTION SET FOR THE HG93C46

Instruction	SB	Op Code	Address		Data		Comments
			X8	X16	X8	X16	
READ		10	A6 -A0	A5 -A0			Reads data stored at specified memory location.
EWEN	1	00	11XXXXX	11XXXX			Write enable command (must be issued before any erase or write operation).
ERASE	1	11	A6 -A0	A5 -A0			Erases memory location An -A0
WRITE	1	01	A6 -A0	A5 -AC	D7 -DO	D15 -DO	Writes to memory location An -A0
ERAL	1	00	10XXXXX	10XXXx			Erases all memory locations.Valid only at Vcc =4.5V to 5.5V
WRAL1		00	01XXXXx	01XXXx	D7-D0	D15 -DO	Writes all memory locations.Valid only at Vcc=4.5V to 5.5VDisables all erase or write instructions
EWDS	1	00	00XXXXX	00xxxx			

Note:The X's in the address field represent don't care values and must be clocked.

INSTRUCTION SET FOR THE HG93C46/56/66

Instruction	SB	Op Code	Address		Data		Comments
			X8	X16	X8	X16	
READ	1	10	A_8-Ao	Az-Ao			Reads data stored at specified memory location.
EWEN	1	00	11XXXXXXX	11XXXXX			Write enable command (must be issued before any erase or write operation).
ERASE	1	11	A_8-Ao	Ar-Ao			Erase memory location An-Ao
WRITE		01	A_8-Ao	Ar-Ao	D_7-D_o	D15-D_o	Writes memory location An-Ao
ERAL	1	00	10xXXXXXx	10XXXXXx			Erases all memory locations. Valid only at Vcc=4.5V to 5.5V
WRAL 1		00	01XXXXXxx	01XXXXX	Dr-Do	D15-Do	Writes all memory locations.Valid only at Vcc=4.5V to 5.5V Disables all erase or write instructions
EWDS	1	00	00XXXXXxx	00XXXxxx			

Note:The X`s in the address field represent don't care care values and must be clocked

FUNCTIONAL DESCRIPTION

The HG93C46/56/66 supports 7 different instructions,which must be clocked serially using the CS,SK and DI pins.Before sending each of these instructions,the CS pin must first be pulled high followed by a START bit (logic'1).The next sequence includes a 2-bit Op Code and usually an 8 or 16-bit address. The next description describes the various functions in the chip.

READ(READ): The Read(READ)instruction includes the Op Code("10")followed by the memory address location to be read. After the instruction and address is sent,the data from the memory location can be clocked out using the serial output pin D0.The data changes on the rising edge of the clock,so the falling edge can be used to strobe the output.

Note that during shifting the last address bit,the DO pin is a dummy bit (logic "0").

ERASEWRITE(EWEN): When the chip is first powered-on,no erase or write instructions can be issued.Only when the Erase/Write Enable (EWEN)instruction is sent will the system be allowed to write to the chip.The EWEN command only needs to be issued once after being powered-on.To disable the chip again,the Erase/Write Disable (EWDS)command can be used.

ERASE(ERASE): The Erase (ERASE)instruction clears the designated memory location to a logical '1' state.After the Op Code and address location is inputted,the chip will enter into an erase cycle.When the cycle completes,the chip will automatically enter into standby mode.

WRITE(WRITE): The Wite (WRITE)instruction is used to write to a specific memory location.If word mode (x16)is selected,then 16 bits of data will be written into the location.If byte mode (x8)is chosen, then 8 bits of data will be written into the location.The write cycle will begin automatically after the 8 or 16 bits are shifted into the chip.

ERASE ALL(ERAL) :The Erase All (ERAL)instruction is primarily used for testing purposes and only functions when Vcc=4.5 V to 5.5 V.This instruction will clear the entire memory array to 1'.

WRITE ALL(WRAL):The Write All (WRAL)instruction will program the entire memory array according to the 8 or 16-bit data pattern provided.The instruction will only be valid when Vcc=4.5 V to 5.5 V.

ERASE/WRITE DISABLE(EWDS):The EraseWrite Disable (EWDS)instruction blocks any kind of erase or program operations from modifying the contents of the memory array.This instruction should be executed after erasing or programming to prevent accidental data loss.

Note also that the READ instruction will operate regardless of whether the chip is disabled from program and write operations.

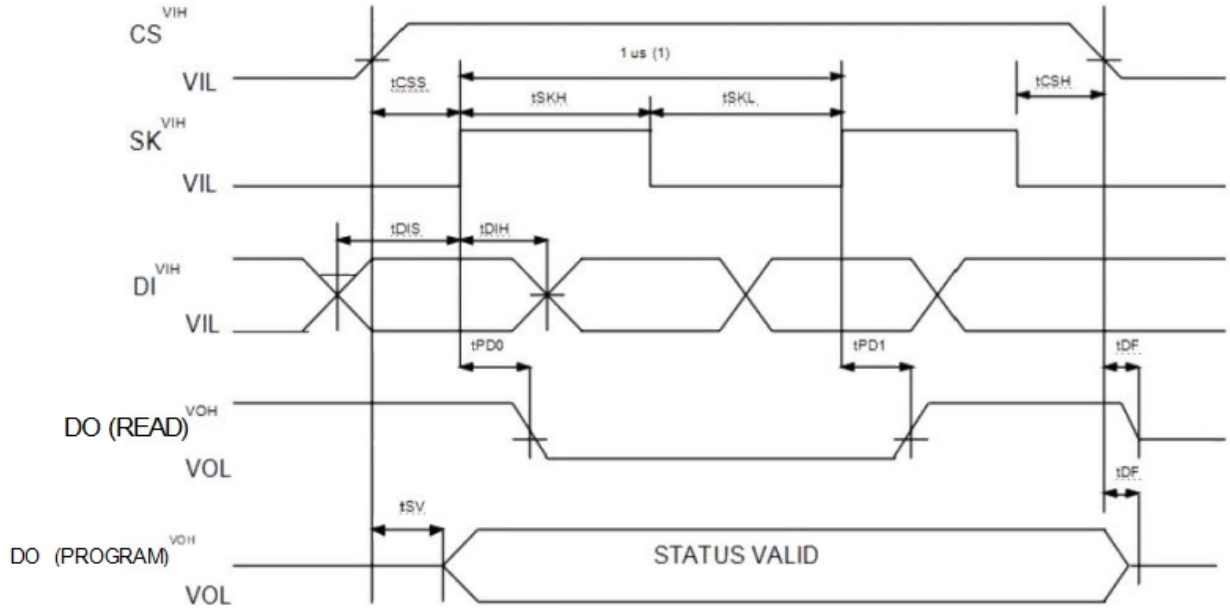
READY/BUSY

To determine whether the chip has completed an erase or write operation,the CS signal can be pulled LOW for a minimum of 250 ns (tcs)and then pulled back HIGH to enter Ready/Busy

mode.If the chip is currently in the programming cycle,tWP,then the DO pin will go low (logical "0").When the write cycle completes,the DO pin is pulled high(logical "1")to indicate that the part can receive another instruction.Note that the Ready/Busy polling cannot be done if the chip has already finished and returned back to standby mode

TIMING DIAGRAMS

Synchronous Data Timing



Note (1):This is the minimum SK period.

ORGANIZATION KEY FOR TIMING DIAGRAMS

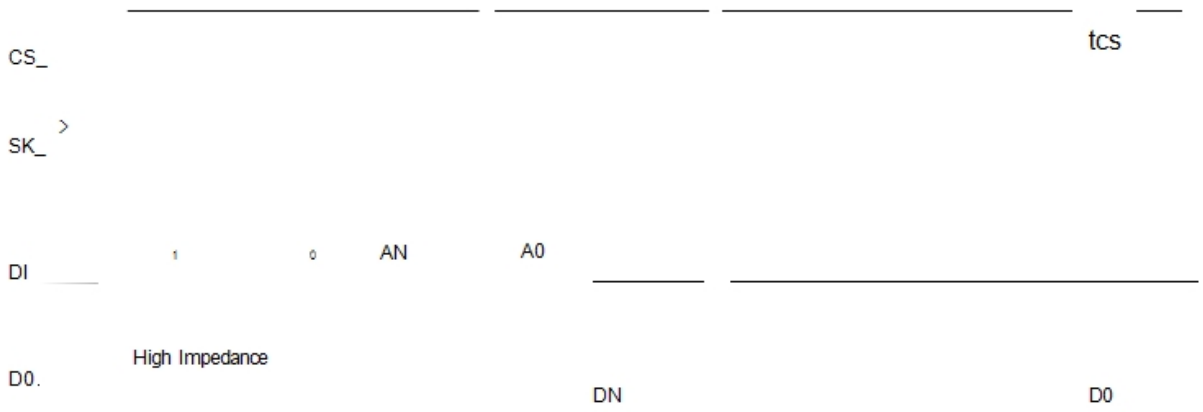
I/O	93C46(1K)		93C56(2K		93C66(4K	
	×8	×16	×8	×16	**×8**	**×16**
AN	As	As	A_8	A_7	A_8	A_7
DN	D_7	D15	D7	D15	D_7	D15

Notes:

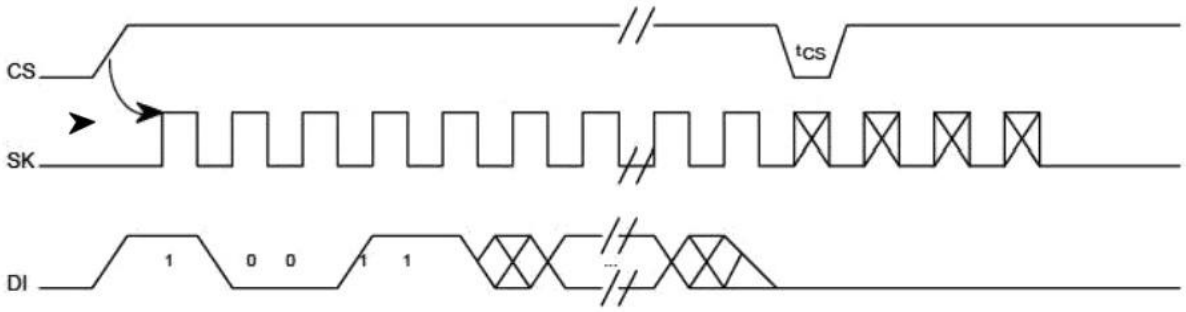
1.Ag is a DON,T CARE value,but the extra clock is required.

2.A7is a DON,T CARE value,but the extra clock is required.

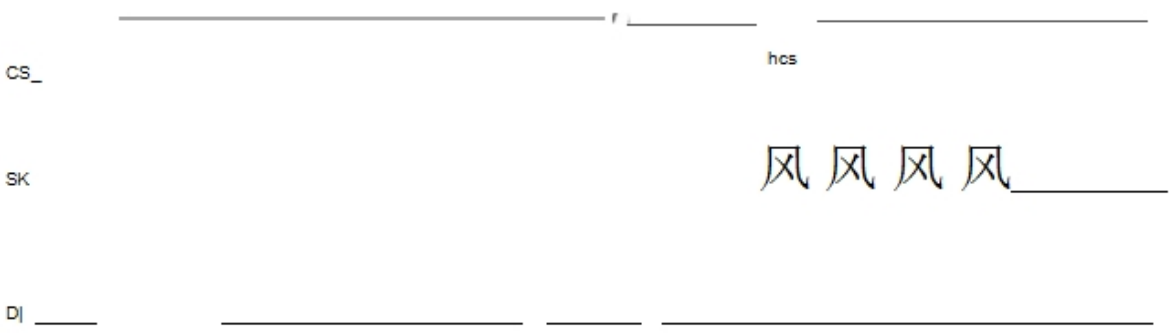
READ TIMING



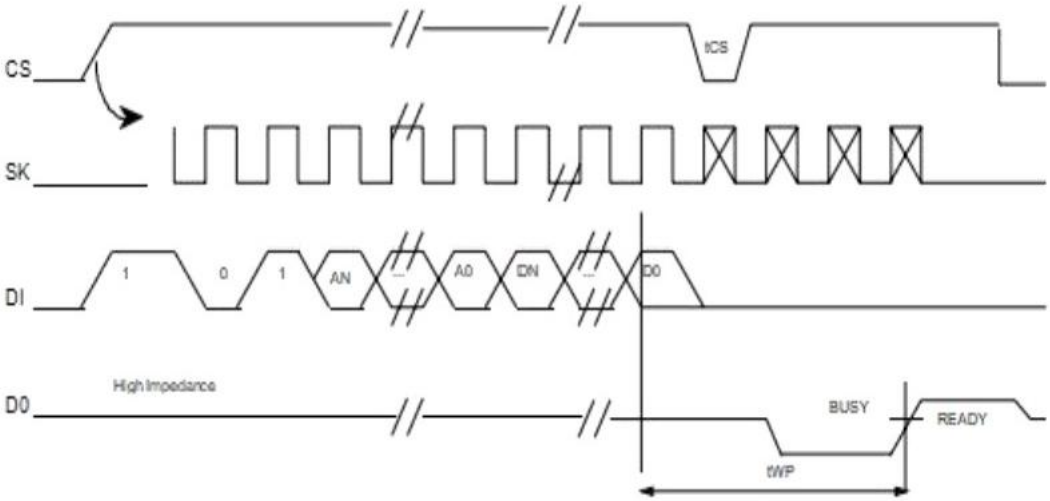
EWEN TIMING



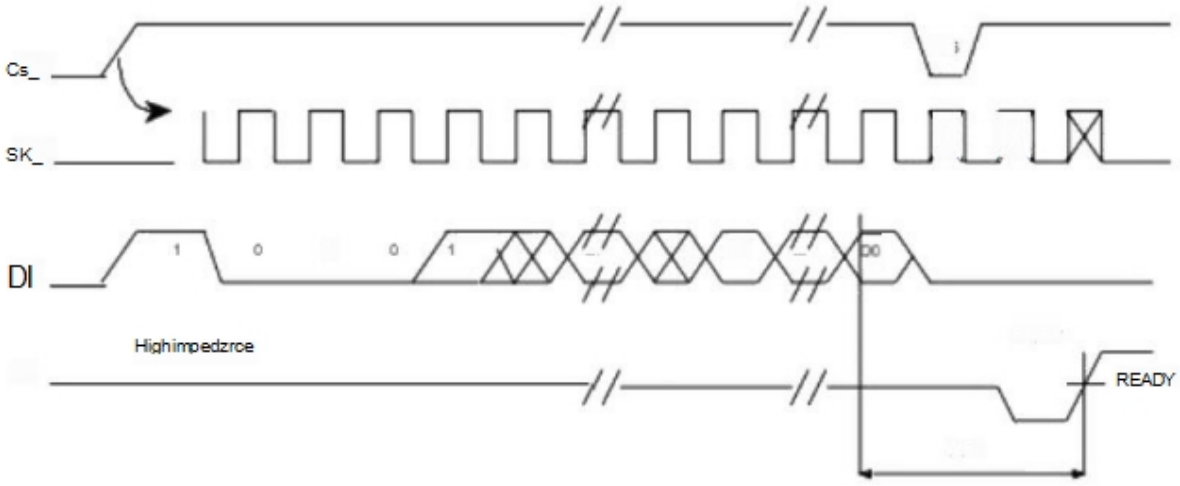
EWDS TIMING



WRITE TIMING

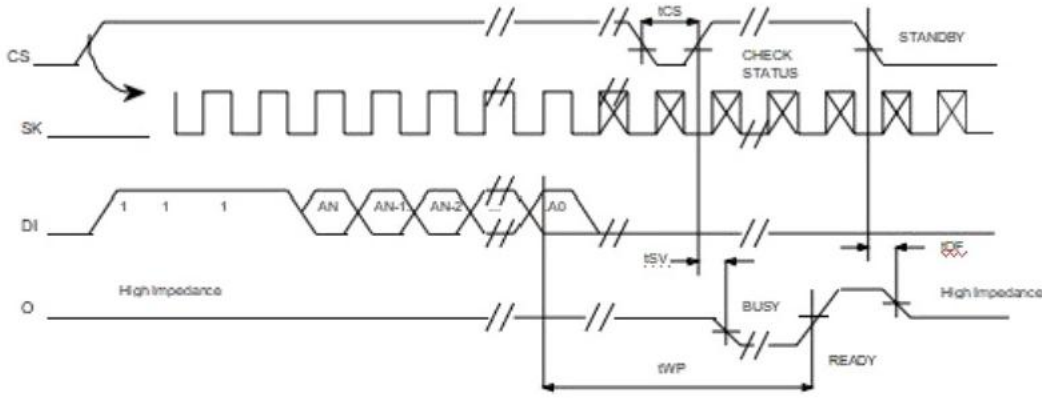


WRAL TIMING"

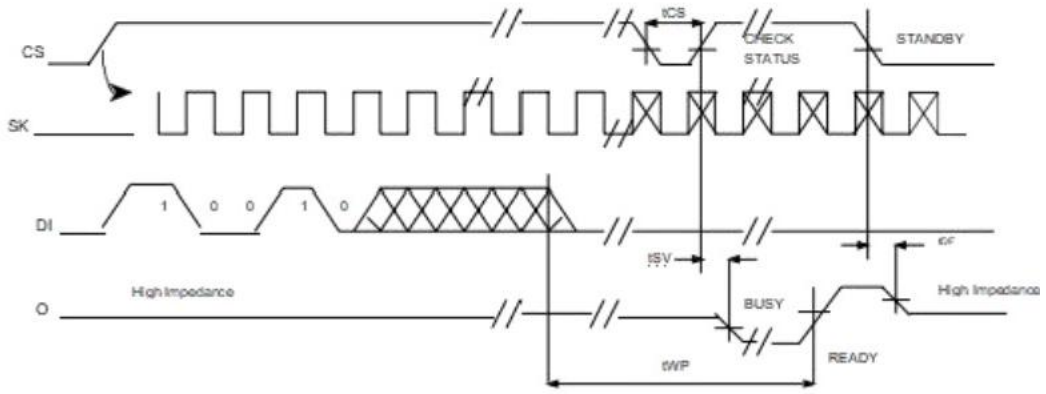


(1)Valid only at Veg=4.5V to 5.5V

ERASE TIMING



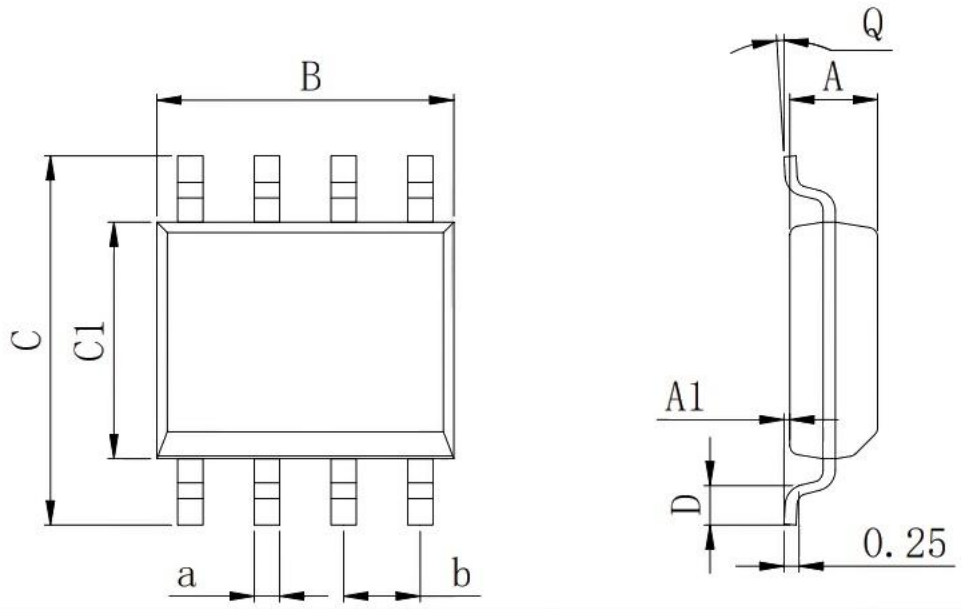
ERAL TIMING”



Valid only at Vcc =4.5V to 5.5V

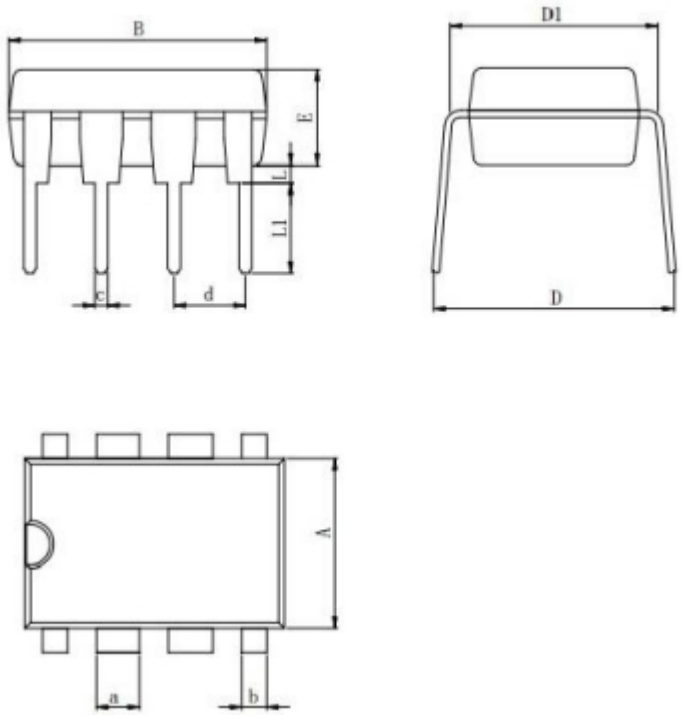
PHYSICAL DIMENSIONS

SOP-8



Dimensions In Millimeters(SOP-8)									
Symbol:	**A**	A1	B	C	**C1**	**D**	Q	a	b
Min:	**1.35**	0.05	4.90	5.80	3.80	**0.40**	0°	0.35	**1.27 BSC**
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

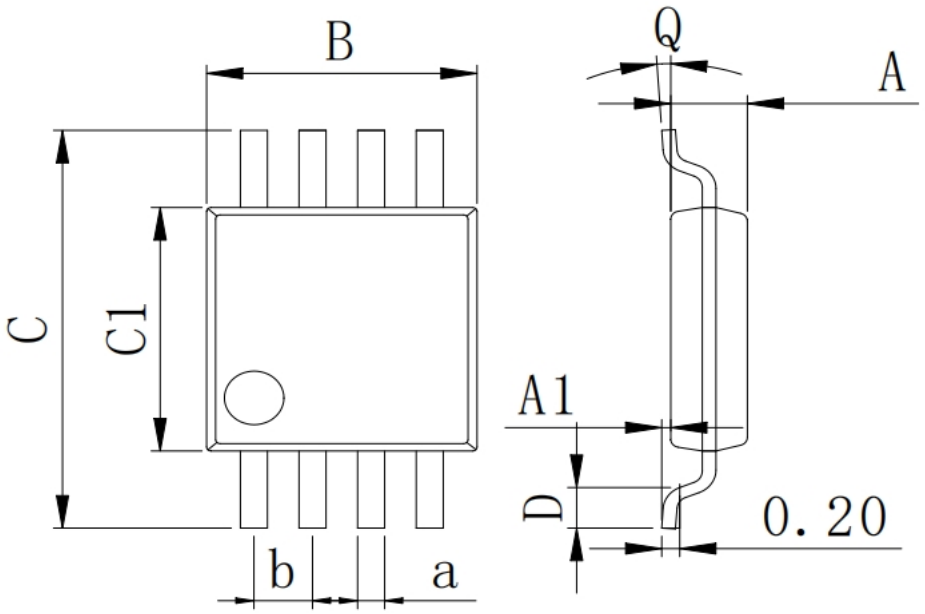
DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	**A**	B	D	D1	E	L	**L1**	**a**	**b**	C	d
Min:	6.10	9.00	8.10	**7.42**	3.10	0.50	**3.00**	**1.50**	**0.85**	**0.40**	**2.54 BSC**
Max:	6.68	9.50	10.9	7.82	3.55	0.70	**3.60**	**1.55**	**0.90**	**0.50**	

PHYSICAL DIMENSIONS

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	**A**	A1	B	**C**	**C1**	**D**	**Q**	a	b
Min:	0.80	0.05	2.90	**4.75**	2.90	0.35	0°	**0.25**	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	**8°**	0.35	