BT134

Rev.E Mar.-2016

描述 / Descriptions

SOT-89 塑封封装双向可控硅。 Triac in a SOT-89 Plastic Package.

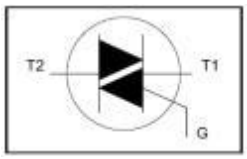
特征 / Features

低功率控制极电路。
Low power gate trigger circuits..

用途 / Applications

一般用于双向转换和增强型控制。
USE in general purpose bi-directional switching and phase control application.

内部等效电路 / Equivalent Circuit



引脚排列 / Pinning

PIN1： Main Terminal 1 PIN 2 ： Main Terminal 1： PIN3: Gate

放大及印章代码 / h_{FE} Classifications & Marking

见印章说明。 See Marking Instructions.

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极限参数 / Absolute Maximum Ratings(Ta=25℃)

参数 Parameter	符号 Symbol	数值 Rating	单位 Unit
Repetitive peak off-state voltages	V_{DRM}	500 600 800	V
RMS on-state current	$I_{T(RMS)}$	1.5	A
Non-repetitive peak on-state current	$I_{TSM(t=20ms)}$	16	A
$I^2t$for fusing	$I^2t_{(t=10ms)}$	1.28	A^2S
Repetitive rate of rise of on-state current after triggering	$dI_T/dt_{(T2+G+)}$	50	A/μS
	$dI_T/dt_{(T2+G-)}$	50	
	$dI_T/dt_{(T2-G-)}$	50	
	$dI_T/dt_{(T2-G+)}$	10	
Peak gate current	I_{GM}	2.0	A
Peak gate voltages	V_{GM}	5.0	V
Peak gate power	P_{GM}	5.0	W
Average gate power	$P_{G(AV)}$	0.5	W
Junction Temperature	T_j	125	℃
Storage Temperature Range	T_{stg}	-40～150	℃

电性能参数 / Electrical Characteristics(Ta=25℃)

参数 Parameter	符号 Symbol	测试条件 Test Conditions		最小值 Min	典型值 Typ	最大值 Max	单位 Unit
Gate trigger current	I_{GT}	V_D=12V I_T=0.1A	I-II-III		1.1	3.0	mA
			IV		4.5	10	
Latching current	I_L	V_D=12V I_{GT}=0.1A	I-III		1.0	5.0	mA
			II-IV		3.0	8.0	
Gate trigger voltage	V_{GT}	V_D=12V I_{GT}=0.1A	I-II-III		0.7	1.5	V
			IV		1.5	2.0	
		V_D=400V I_T=0.1A	T_j=125℃	0.2	0.3		
Holding current	I_H	V_D=12V	I_{GT}=0.1A		0.8	5.0	mA
On-state voltage	V_T	I_T=1.5A			1.2	1.5	V
Off-state leakage current	I_D	$V_D=V_{DRM(max)}$	T_j=125℃		0.1	0.5	mA

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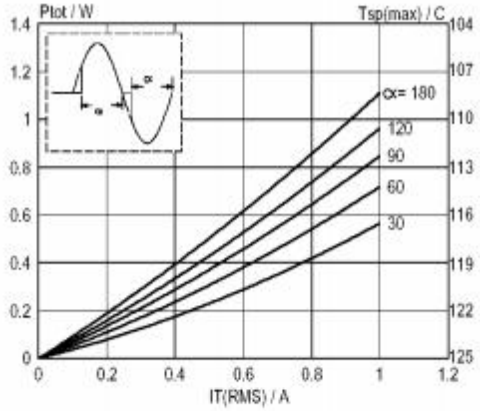
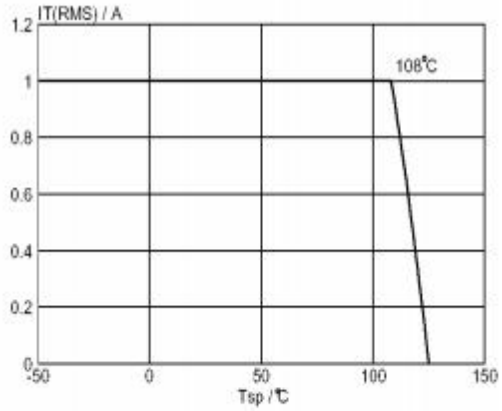
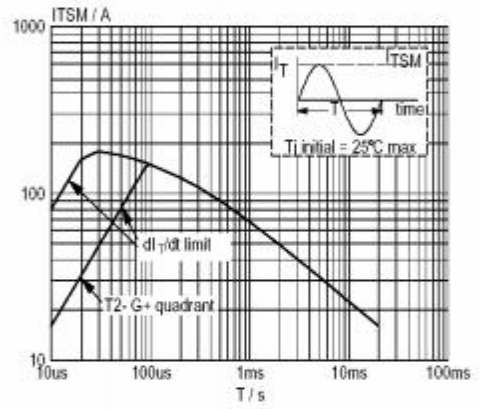
电参数曲线图 / Electrical Characteristic Curve



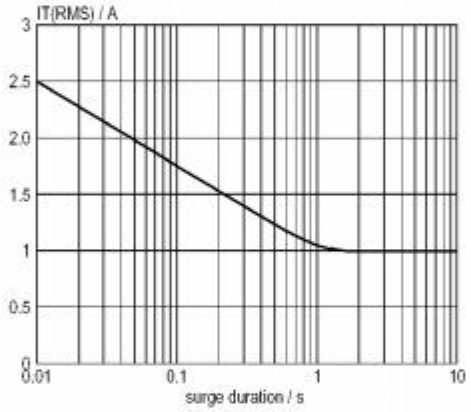
Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.



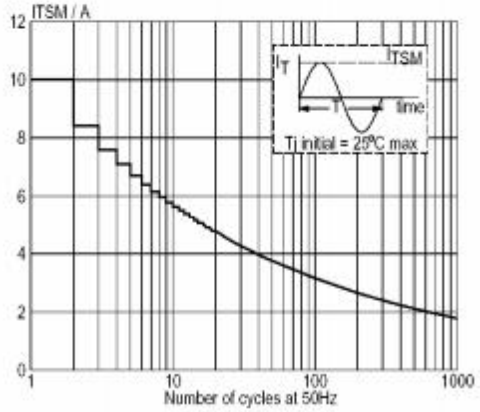
Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature T_{lead}.



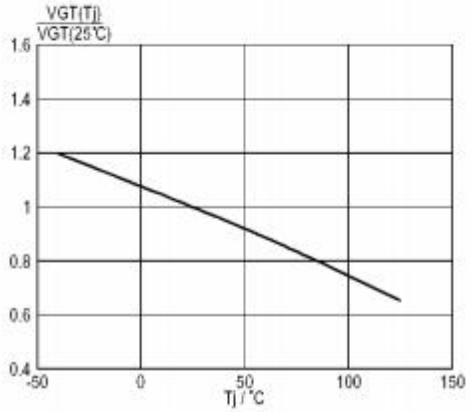
Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.



Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{lead} \leq 51°C$.



Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.



Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.