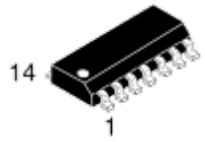
General Description

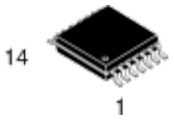
CD4073B, CD4081B and CD4082B AND Gates.provide the system ed

Inner with direct implementation of the AND function and supplement the existing family of CMOS gates.

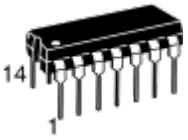
The CD4073B , CD4081B , and CD4082B types are supplied in 14-lead DIP package, 14-lead SOP package, AND 14-lead TSSOP 15- package.



SOP-14



TSSOP-14



DIP-14

Features

- Medium-Speed Operation -TPLH, TPHL=60ns （tsp.at VDD =10 V
- 100% tested for quiescent current at 20V Maximum input current of 1μA at 18 V over full pack-temperature range, 100 nA at 18 V and 25° C
- Noise margin （full package-temperature range）
  - 1V at VDD=5V
  - 2V at VDD= 10V
  - 2.5V at VDD= 15V
- Standardized,symmetrical ou taut characteristics
- 5V、 10Vand 15V parametric ratings
- Meets all requirements of JEDEC Tentative Tankard No. 13B, Standard Specifications

Order Information

Device	Package Type	Marking	Packing	Packing Qty
CD4073BE/ CD4073BN	DIP-14	CD4073B	TUBE	1000pcs/box
CD4073BM/TR	SOP-14	CD4073B	REEL	2500pcs/reel
CD4073BMT/TR	TSSOP-14	CD4073B	REEL	2500pcs/reel
CD4081BE/ CD4081BN	DIP-14	CD4081B	TUBE	1000pcs/box
CD4081BM/TR	SOP-14	CD4081B	REEL	2500pcs/reel
CD4081BMT/TR	TSSOP-14	CD4081B	REEL	2500pcs/reel
CD4082BE/ CD4082BN	DIP-14	CD4082B	TUBE	1000pcs/box
CD4082BM/TR	SOP-14	CD4082B	REEL	2500pcs/reel
CD4082BMT/TR	TSSOP-14	CD4082B	REEL	2500pcs/reel

Maximum Ratings,Absolute-Maximum Values:

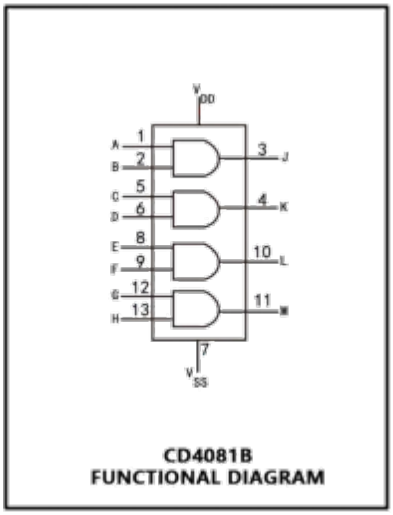
Parameter	Value	Unit
Voltages Reference To Vss Terminal	-0.5 to +20	V
Input Voltage Range,Allinputs	-0.5 to VDD + 0.5	V
Dc Input Currentany One Input	±10	mA
Power Dissipation Per Package(Pd)：		
For Ta=55℃To +100℃	500	mA
For Ta=+100℃ To +125℃	2mW/°C to 200	mW
Device Dissipation Per Output Transistor		
For Ta -Full Package-Temperature Range (Al Package Types)	100	mW
Operating-Temperature Range(Ta)	-40 to +85	°C
Storage Temperature Range (Stag)	65 to +150	°C
At Distance 1/16± 1/32inch(1.59+0.79mm)From Case For 10s Max	+245	°C

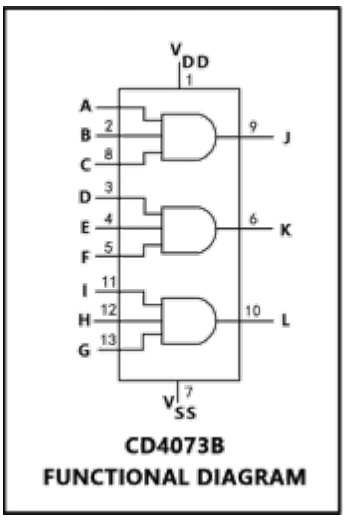
Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

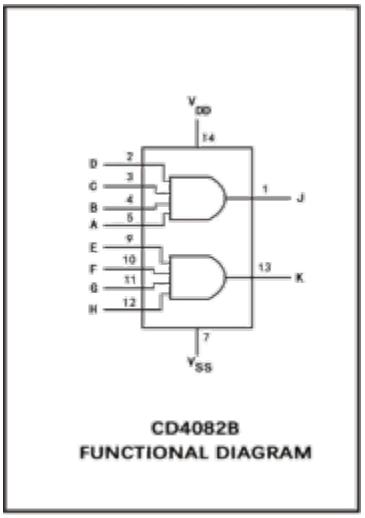
Recommended operating conditions

For maximum reliability. nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (for T=Full Package Temperature Range)	5	15	V







Dynaic Electrical Charactetistics

at TA=25°C，Input tr，ft=20ns，and CL=50 pf，RL=200KΩ

CHARACTERISTIC	TEST CONDITIOS VDD Volts		ALL TYPES LIMITS		UNITS
			TYP.	MAX.	
Propagation Delay Time,TPHL,TPLH		5 10 15	125 60 40	250 120 90	NS
Transition Time, TPHL,TPLH		5 10 15	100 50 40	200 100 80	NS
Input Capacitance,CIN	Any Input	-	5	7.5	Pf
CHARACTERISTIC	TEST CONDITIOS VDD Volts		ALL TYPES LIMITS		UNITS
			TYP.	MAX.	
Propagation Delay Time,TPHL,TPLH		5 10 15	125 60 40	250 120 90	NS
Transition Time, TPHL,TPLH		5 10 15	100 50 40	200 100 80	NS
Input Capacitance,CIN	Any Input	-	5	7.5	Pf

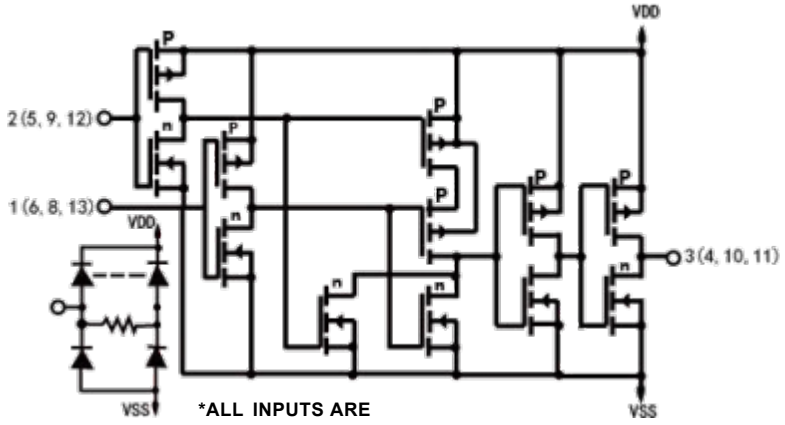


Fig.1 - Schematic for CD4081B （1of4identical Gates）

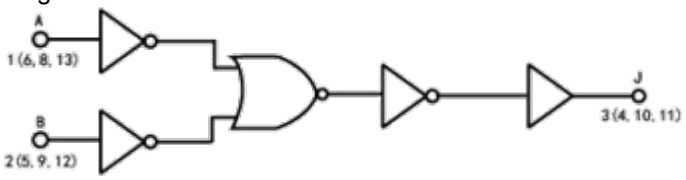


Fig.2 - Logic diagram for CD4081B (1 of 4 identical gates)

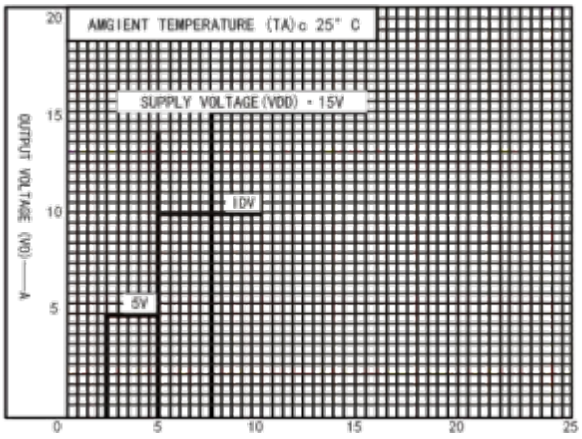


Fig.3-Typocalvoltagetransfercharacteristic.

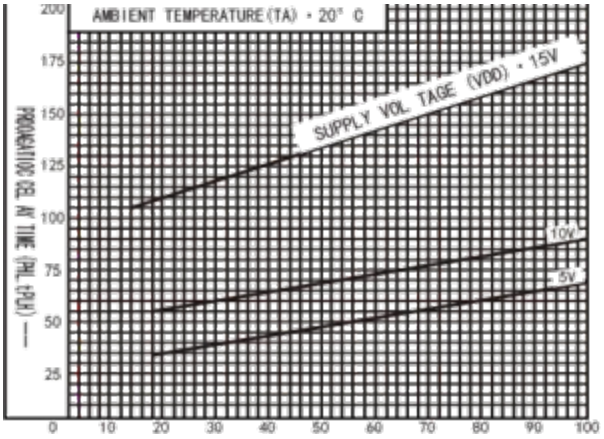


Fig.4 - Typical propagation delay time as afunction of load capacitance.

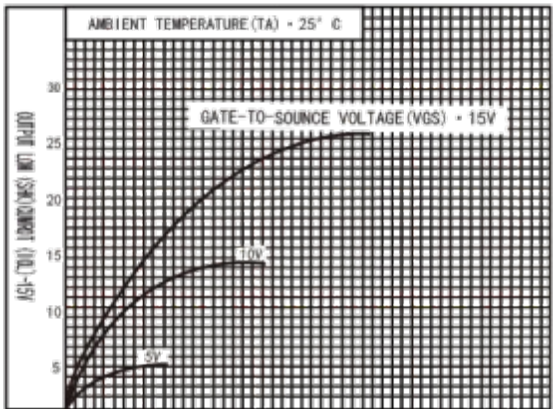


Fig.5 - Typical output low （sink）

Current characteristics.

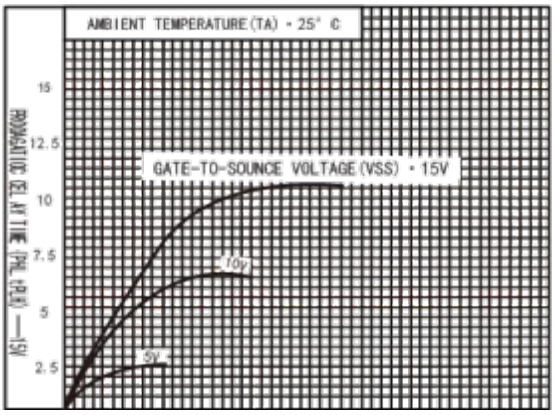


Fig.6 - Minimum output low (sink)

current characteristics.

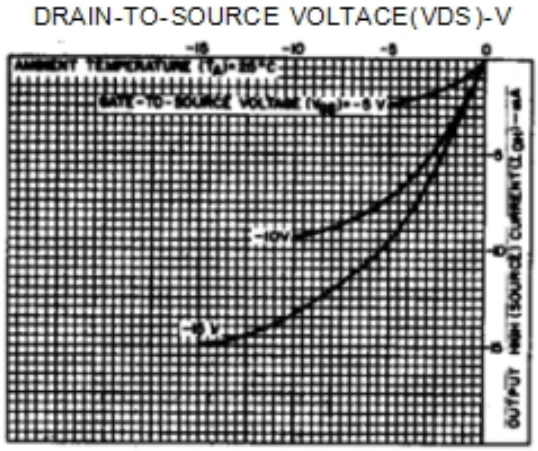


Fig.7 -Minimum output high （source）

current characteristics

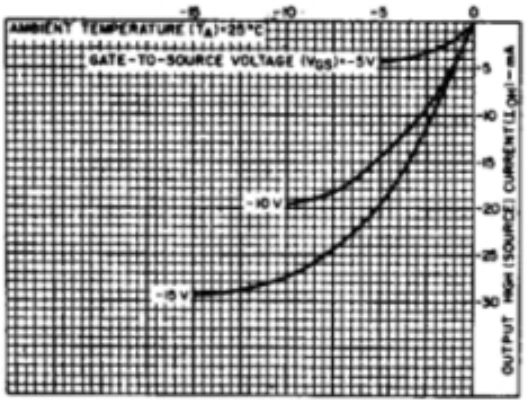


Fig.8 - Typical output high (source)

current characteristics.

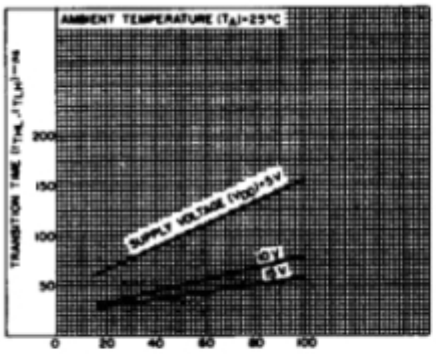


Fig.9 -Typical transition time as a function of load capacitance

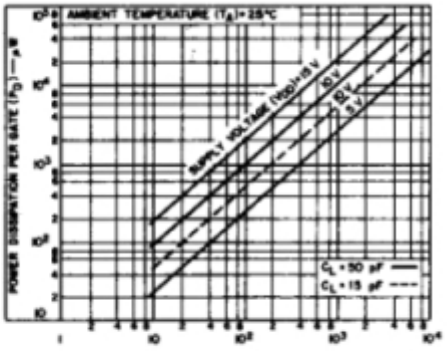


Fig.10 -Typical dynamic power diss i-Ration per gate as a function

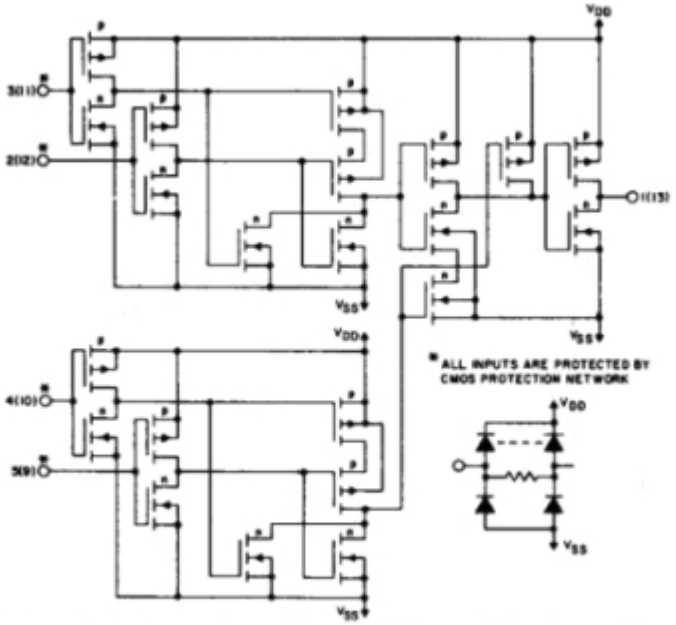


Fig.11 - Schematic diagram for CD4082B(1 of 2identical gates).

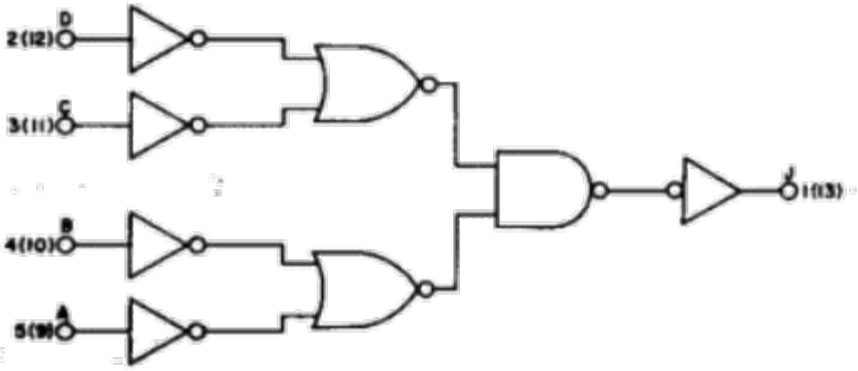
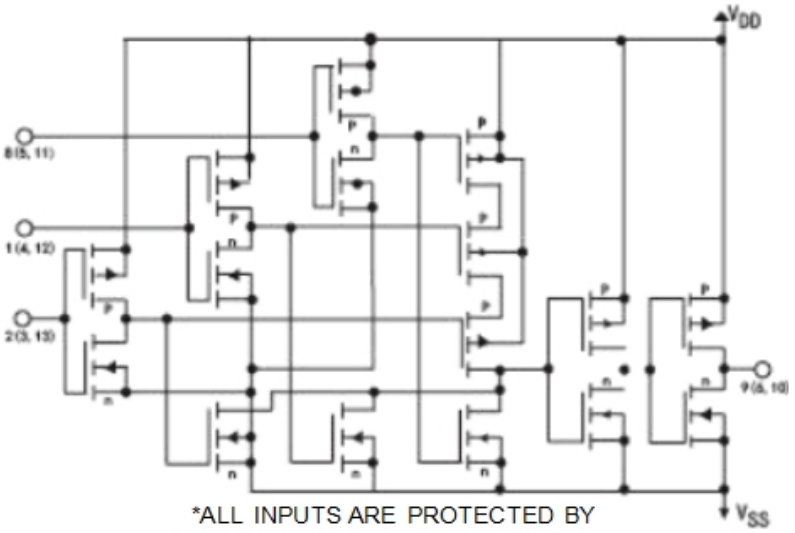


Fig.12 - Logic diagram for CD4082B (1 of 2 identical gates).



*ALL INPUTS ARE PROTECTED BY
CMOS PROTECTION NETWORK

Fig.13 — Logic diagram for CD4073B(1 of 3 identical Gates).

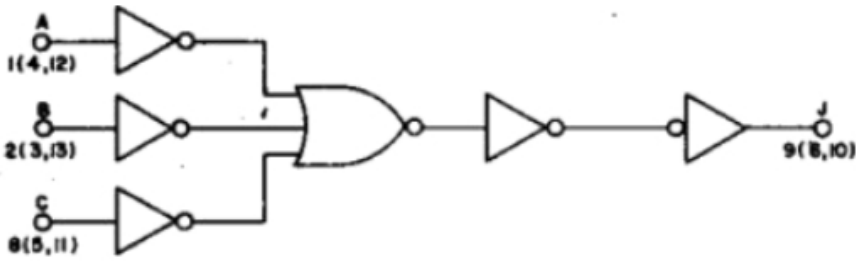


Fig.14 - Logic diagram for CD4073B(1 of 3 identical Gates).

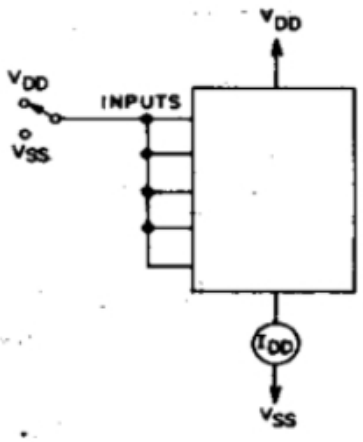


Fig.15 - Quiescent device current test circuit.

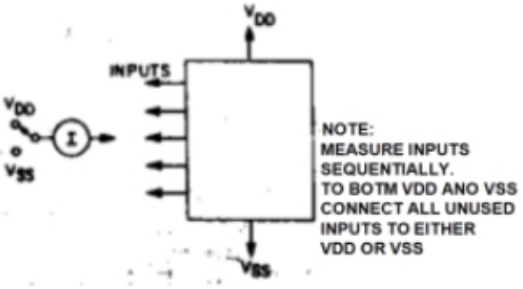


Fig.16 - Input current test circuit.

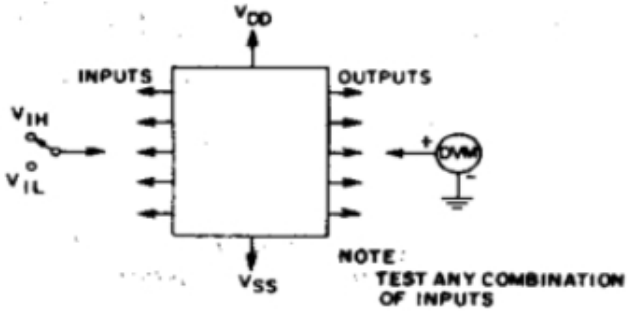
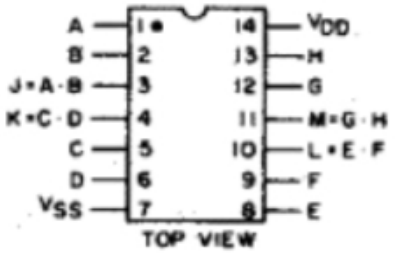
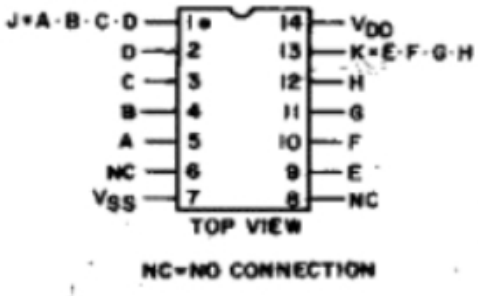


Fig.17 - Input-voltage test circuit.

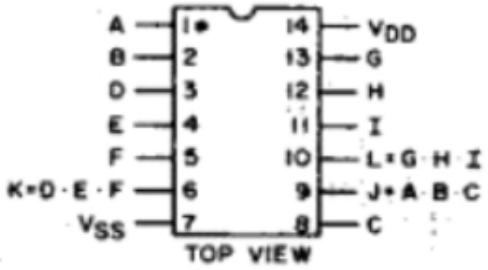
TERMINAL ASSIGNMENTS



CD4081B



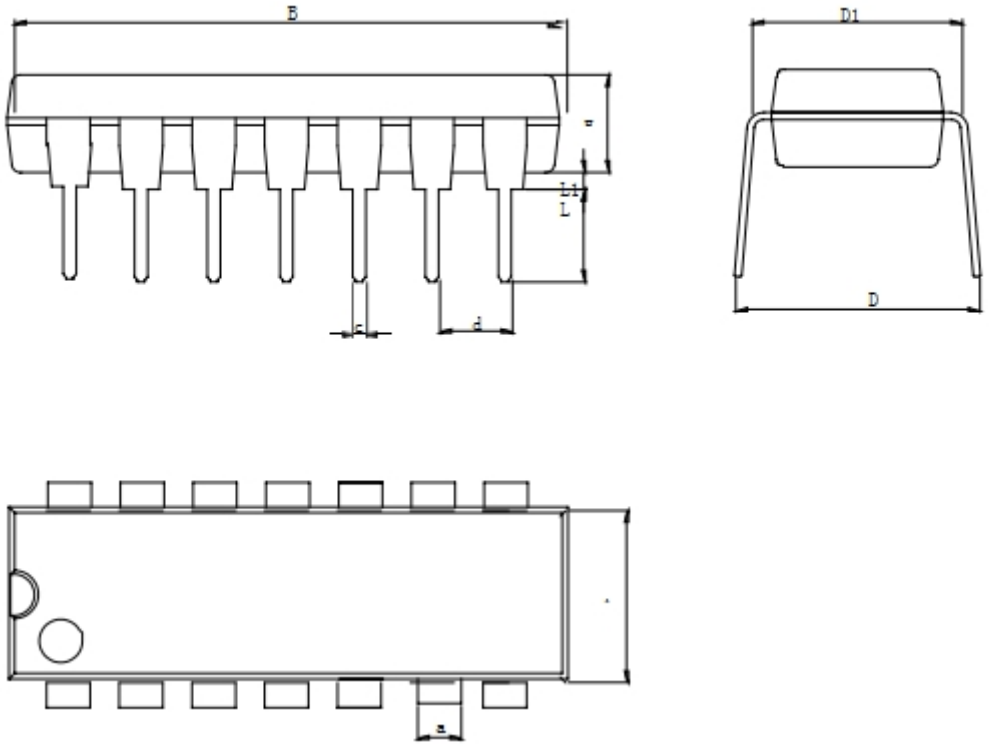
CD4082B



CD4073B

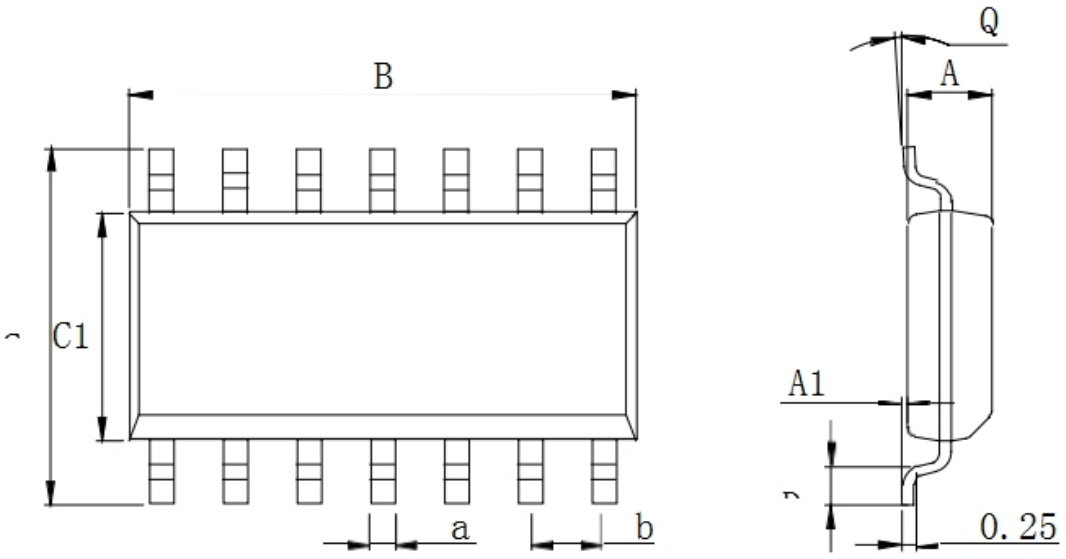
Physical Dimensions

DIP-14



Dimensions In Millimeters(DIP-14)										
Symbol :	A	B	D	D1	E	L	L1	a	c	d
Min :	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max :	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

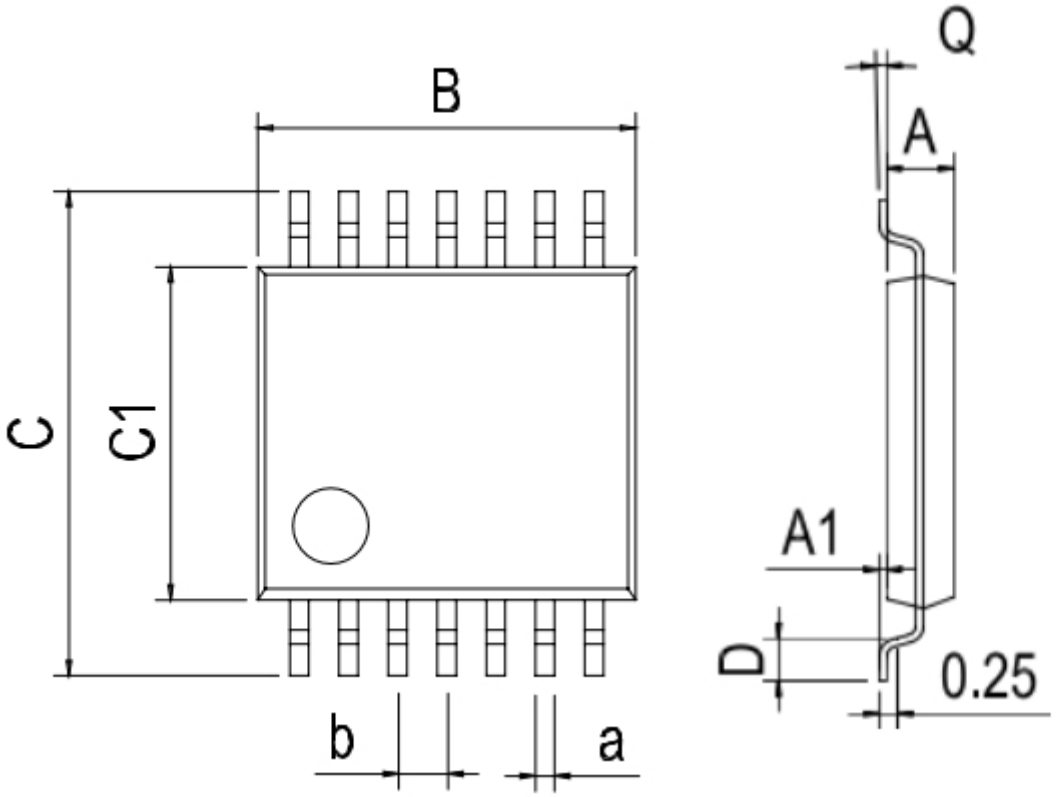
SOP-14



Dimensions In Millimeters(SOP-14)									
Symbol :	A	A1	B	C	C1	D	Q	a	b
Min :	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max :	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol :	A	A1	B	C	C1	D	Q	a	b
Min :	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max :	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	